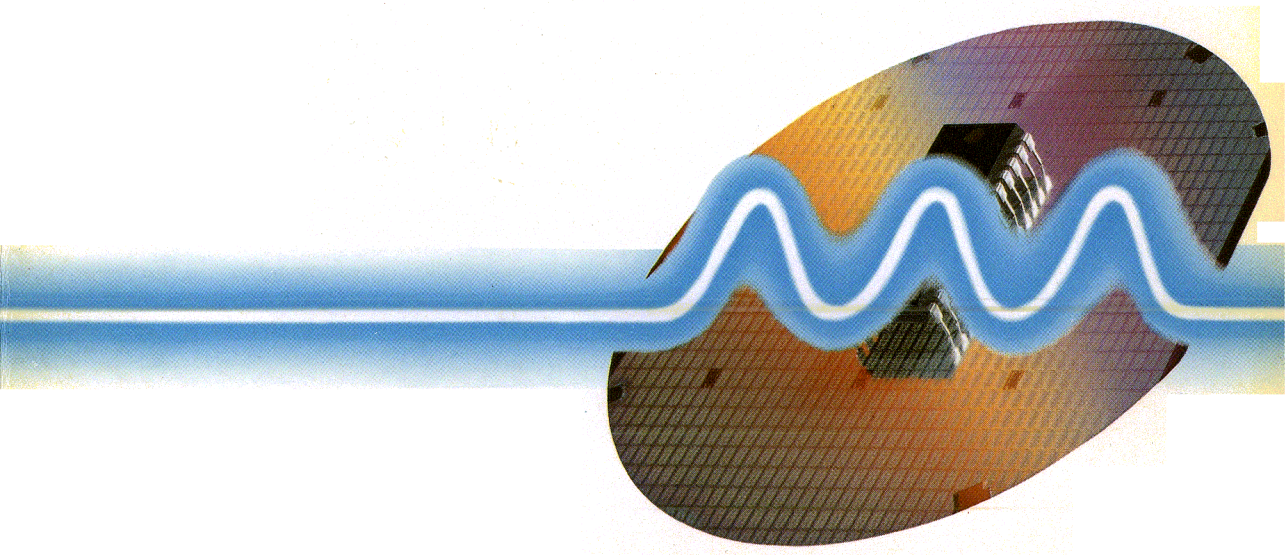
TEXAS INSTRUMENTS

ADVANCED LINEAR EUROPEAN SEMINARS

FOR PRECISION DESIGN OF THE 90'S



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TEXAS INSTRUMENTS

EUROPEAN DESIGN SEMINAR 1990

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Acknowledgements are expressed to the following for their assistance in the organising and production of this series of Linear Design Seminars:
Bridget Marshall, Brian Burke, David Slatter, Active Graphics and Bird Marketing/Design.

IMPORTANT NOTICE

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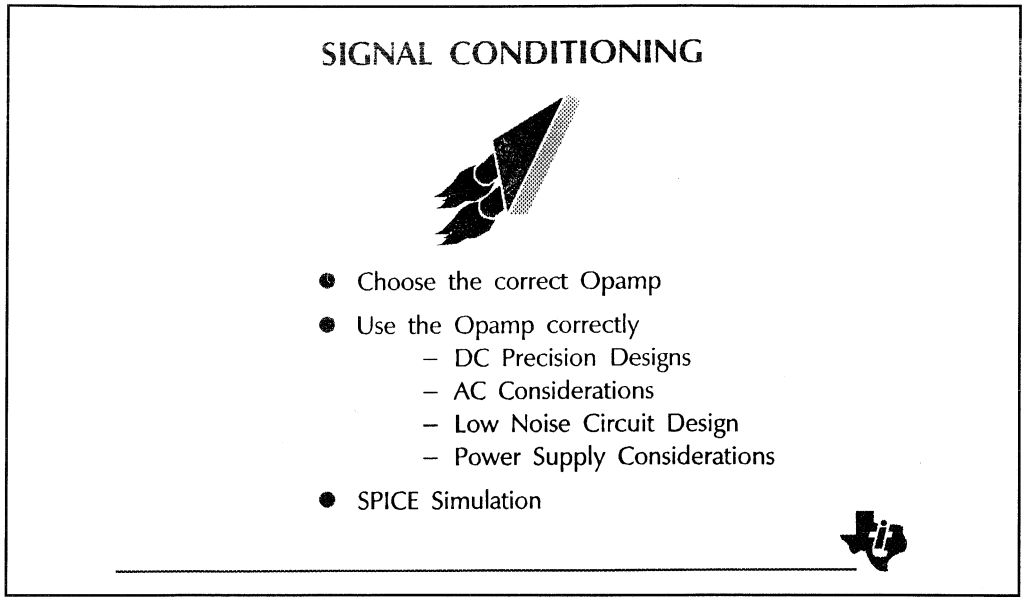
SECTION 1.
SIGNAL CONDITIONING

SIGNAL CONDITIONING INDEX



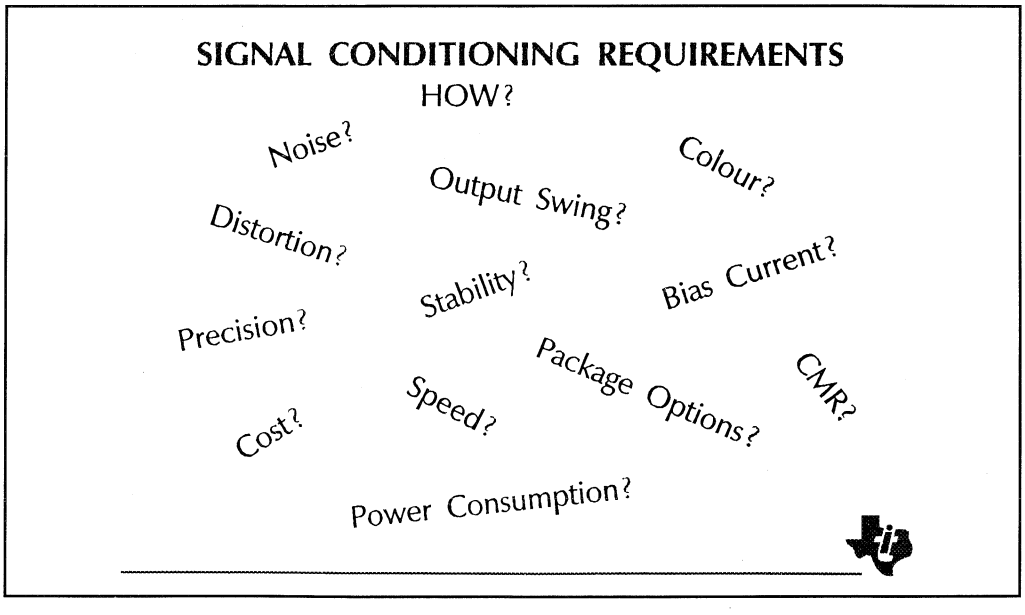


Figure 2 - The op amp selection problem

Choosing the most suitable op amp for a particular circuit out of the thousands available is not a simple task. The aim of this section is to make the selection task easier. Often the choice is limited by many constraints, such as the available power supplies or by the speed of operation. These parameters can be found on any op amp data sheet. However, when choosing an op amp for a precision application the choice is less simple.

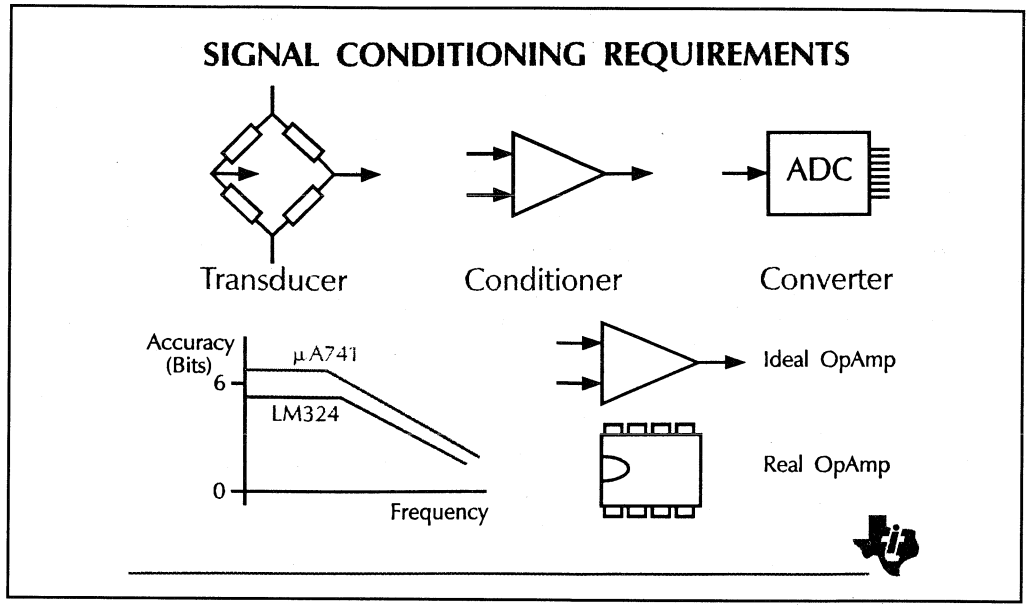


Figure 3 - Signal conditioning system

When designing a total signal processing system from sensor to microprocessor, the error in the analogue - digital conversion is usually the focal point for determining total system accuracy. Often less attention is paid to the signal path from transducer to ADC. However many commodity op amps have only modest performance if all error terms are considered. Several parameters limit precision. Here we will introduce a method of evaluating the performance of op amps by relating accuracy to digital bits.

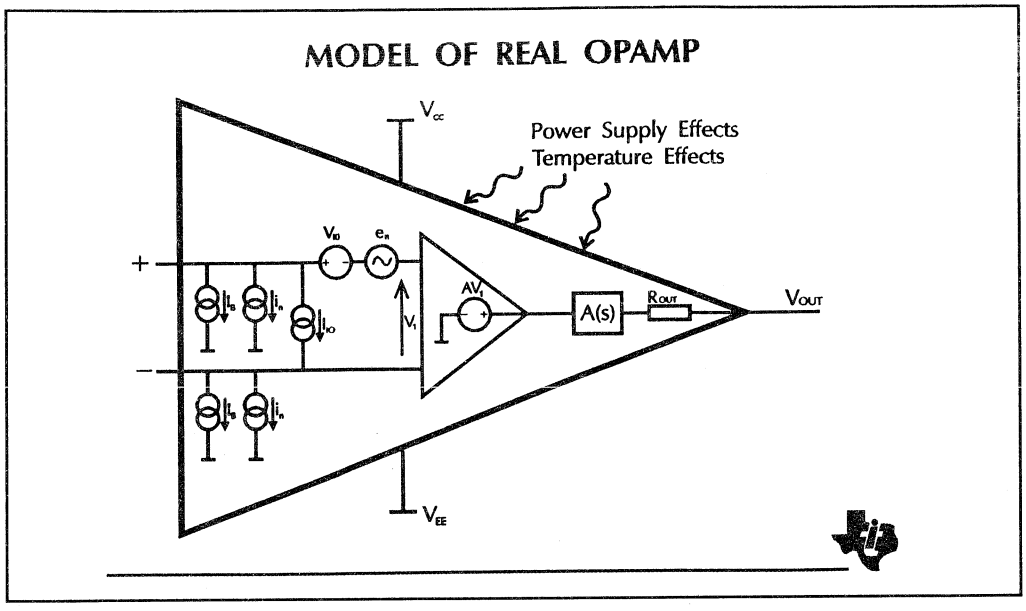


Figure 4 - The real op amp

A real op amp has many non-ideal parameters. The input voltage offset causes a DC ouput error. The input bias currents cause a similar effect due to the additional voltage drop across input source impedances. The voltage and current noise sources limit resolution and dynamic range. The open loop response limits accuracy at high frequencies. The finite slew rate limits settling times. Temperature effects cause changes in the operation of the op amp at different temperatures or while the op amp is warming up.

The dominant error sources which limit the achievable precision may be combined mathematically into a single figure of merit. This number can then be related to the accuracy of digital systems.

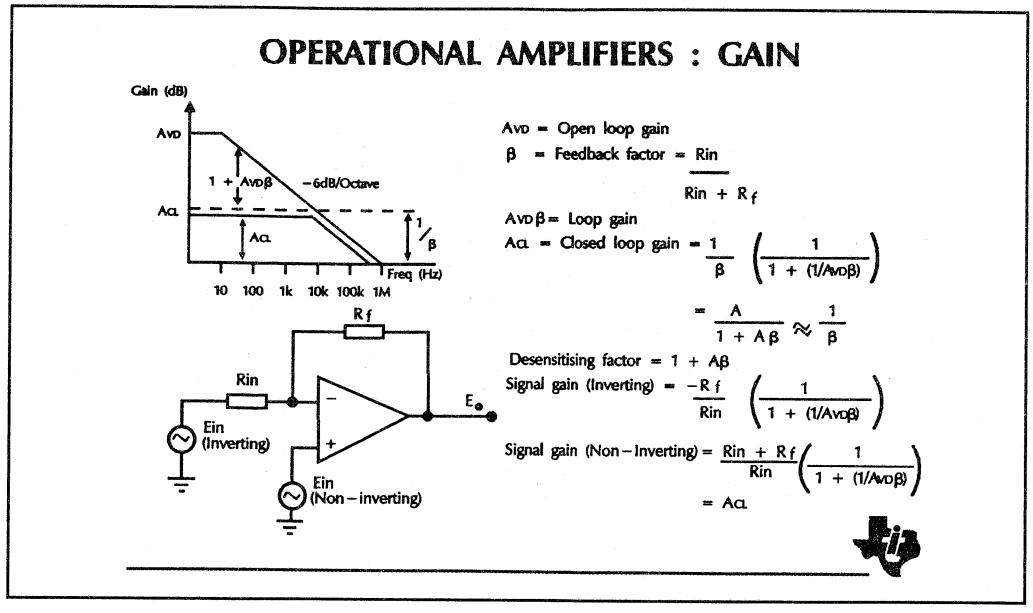


Figure 4A - Operational Amplifier Gain - A Reminder

This slide has been included to act as a reminder about some of the key parameters related to the open loop and closed loop gain of an operational amplifier.

Every op amp has a particular open loop gain, A_{VD}. Ideally this parameter would be infinite, but in reality it will typically be 100dB at DC and rolls off at frequencies above 100 Hz. The frequency at which A_{VD} reaches 0dB is known as the Unity Gain Bandwidth of the Amplifier. The gain limits the accuracy of an op amp and the bandwidth limits the maximum operating frequency.

To use an op amp feedback will be used to give the device a particular Closed Loop Gain, A_{CL}. This feedback actually improves an op amp's performance by making it behave more like the ideal device - it improves parameters such as input impedance, output impedance and distortion.

The amount by which feedback improves an op amp's performance is dependant upon the difference between the closed loop and open loop gains. At low frequencies this difference, ' 1+Aß ' is large and the op amp performs well, at higher frequencies is smaller and therefore the input impedance, output impedance etc are all degraded. It is therefore important to ensure that ' 1+Aß ' is always large at the maximum operating frequency of the op amp circuit.

The closed loop gain is the gain by which errors on the input are multiplied to see their effect on the output. For example, Vio and En are multiplied by A_{CL} to see the error on the output.

It must be remembered that the closed loop gain is often different to the signal gain. For an inverting amplifier the input signal is multiplied by the signal gain and not the closed loop gain to see what effect it has on the output.

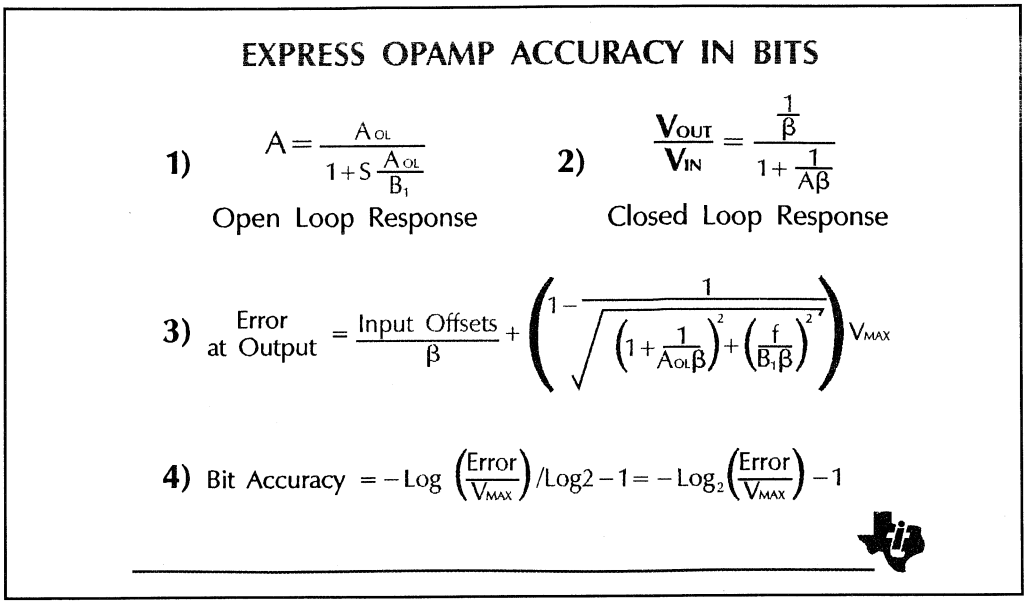


Figure 5 - Bits of accuracy

A	Open Loop Response of Op Amp	f	Frequency
A_{VD}	DC gain of Op Amp	S	Complex Frequency Variable (= j 2 π f)
ß	Feedback Factor	V_{MAX}	Voltage Range at Output
B1	Unity Gain Bandwidth of Op Amp		

The accuracy of an amplifier is typically limited by two parameters - the non-zero offsets and the finite open loop gain. The offsets arise from the offset voltage of the op amp and the voltage drop across the resistors due to non-zero bias currents. Ideally, both offsets would be zero. At high frequencies, the accuracy becomes limited by the finite gain of the op amp. Because the open loop gain of the op amp rolls off with frequency, so does the accuracy.

The gain error is calculated by considering how the open loop response of the op amp affects the closed loop response. The open loop response is modelled with a simple first order reponse and this equation (1) combined with the standard negative feedback equation (2) to give the overall transfer function. The error is taken to be be the difference in magnitude of the ideal output and the real output (3). This is then converted into bits by a simple log (base 2) relationship (4).

This equation only takes into account the open loop gain, bandwidth and offset voltage. Other parameters which might be important in some applications could be added. eg. bias current, offset current, CMRR, k_{SVR} (PSRR), voltage noise, current noise.

The easist way to understand what the equations mean, is to use a computer to plot out graphs.

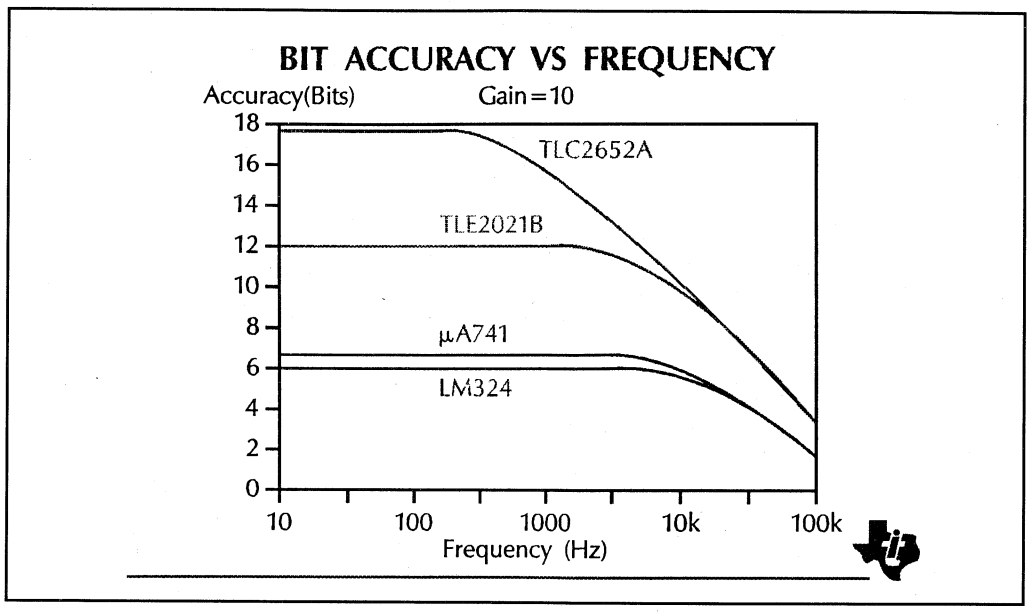


Figure 6 - Graph of bit accuracy vs frequency

The above graphs show the accuracy against frequency for four opamps; the general purpose LM324 and mA741, and the precision TLE2021B and TLC2652A.

The graphs were plotted with the help of a spreadsheet program and using data sheet values for DC gain (min @ 25°C), bandwidth (typ @ 25°C), and offset voltage (max @ 25°C).

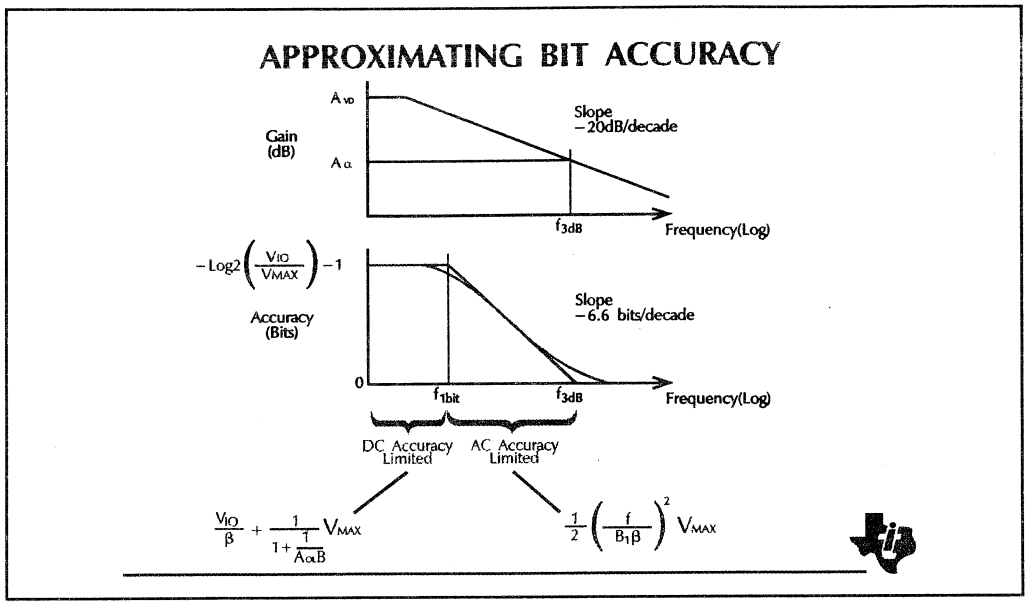


Figure 7 - Bit accuracy approximations

The equation presented above is best graphed with the help of a computer. However it is possible to make approximations with only a few "back of an envelope" calculations.

The value of the bits of accuracy equation is dominated by different parameters over different frequency ranges. At low frequencies the accuracy is limited by DC paramters - the offsets and DC open loop gain. At higher frequencies the accuracy rolls off to almost zero at the -3dB frequency.

7.1 Method for drawing an approximated bit accuracy vs frequency graph.

1. Determine the DC accuracy in bits. This is often limited by the offset voltage.

2. Determine the -3dB point. This is simply the bandwidth multiplied by ß. This frequency equates to the zero bit accuracy frequency in the approximation.

3. Draw the graph!

The frequency where the accuracy rolls off can be found by solving the two equations for f. This can make drawing the graph easier.

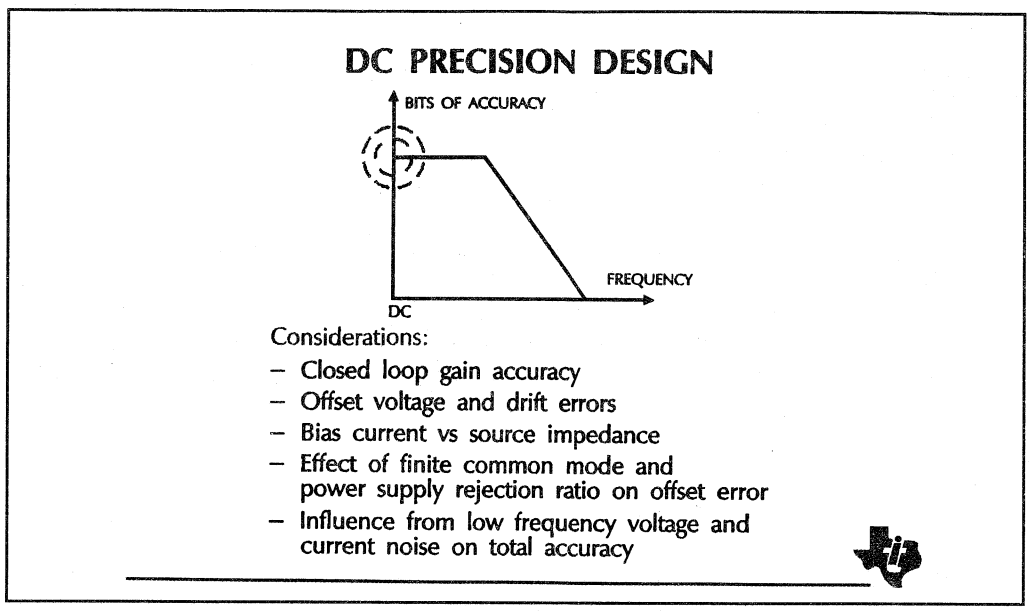


Figure 8 - DC precision design

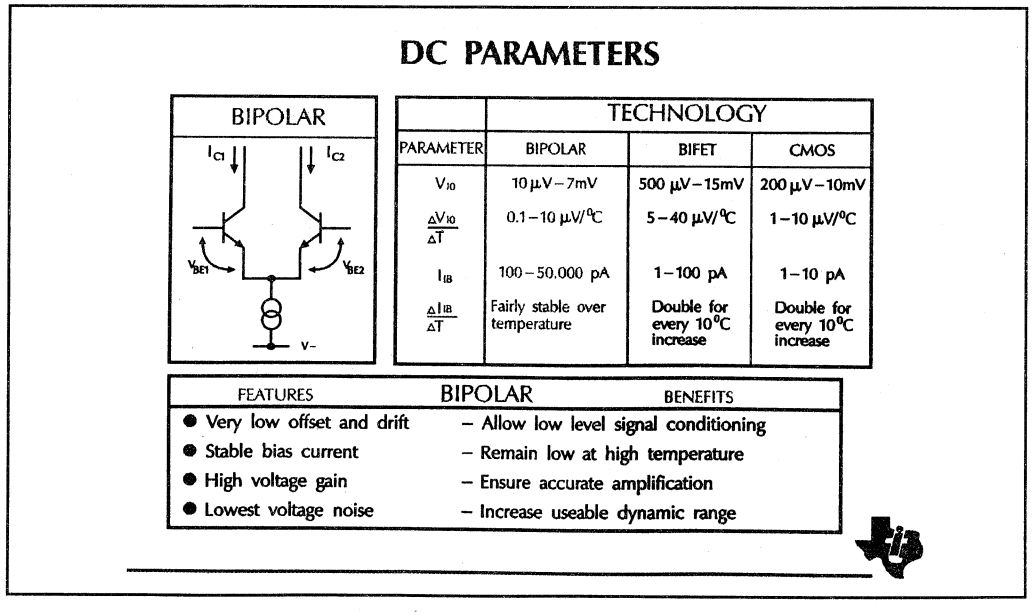


Figure 9 - Bipolar op amps

9.1 Input offset voltage

Offset voltage is mainly due to Vbe mismatch of the input transistors in the op amp's differential input stage. However, variations in the two collector currents also contribute to the total offset. High performance opamps can today offer an offset down to 10µV max @ 25°C.

9.2 Input offset voltage drift

The major cause of offset drift with temperature is:

a) V_{be} mismatch, which can be approximated by:

$$\frac{dV_{IO}}{dT} = \frac{V_{IO}}{T}$$; where T is the absolute temperature in Kelvin.

This direct relation between the absolute offset and its temperature drift means that a V_{IO} = 1mV contributes 3.4μV°C drift. If the offset is trimmed to a minimum the drift will also be reduced.

b) IC mismatch, which can be approximated by:

$$\frac{dV_{IO}}{dT} = (200\mu V/°C) \cdot \log \frac{I_{C1}}{I_{C2}}$$

A 1% collector current mismatch gives less than 1μV/°C drift.

Offset drift with time is low for bipolar input stages. The newly developed Excalibur process has enabled devices (TLE202X family) that achieve a typical V_{IO} drift of just 6nV/month typ.

9.3 Input bias current

Many techniques can be used to reduce the relatively high input bias currents of bipolar op amps. Bias current cancellation circuits can be used, as in devices such as the TLE2027. Alternatively, superbeta NPN input transistors will reduce the input bias currents to FET levels, and keep them low even at high temperatures. The variation in the input bias current is usually proportional with temperature, eg:

$$\frac{dI_b}{dT} = C \cdot I_{IB}$$; where C is a small constant (<<1)

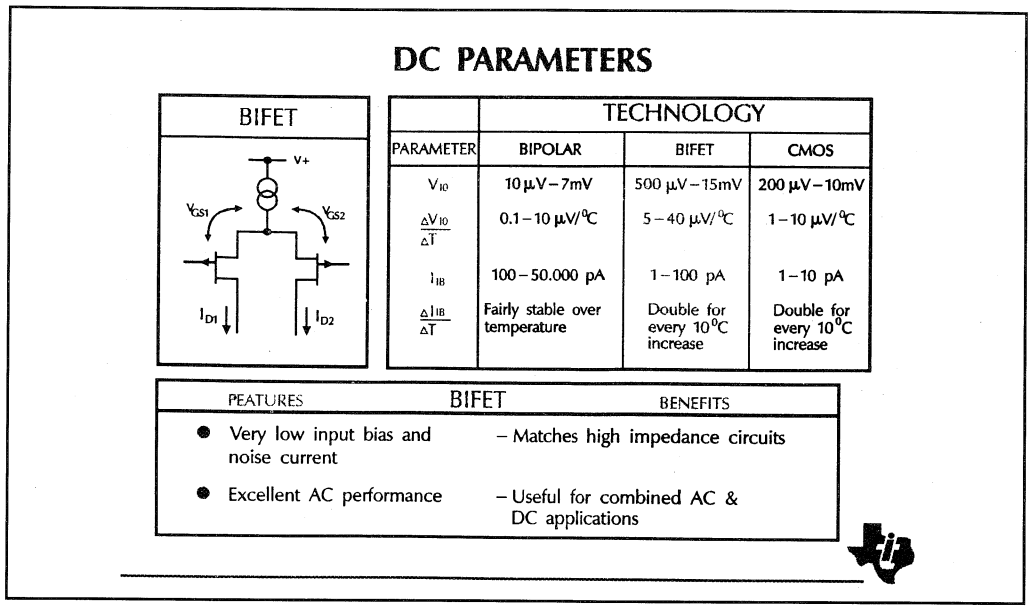


Figure 10 - Bifet op amps

10.1 Input offset voltage

Bifet opamps have typically far greater offsets when compared to bipolar devices. Less uniform DC characteristics and thermal drift make FET matching more difficult and less accurate.

FET input op amps are available today with a few hundred microvolts offset voltage @ 25°C, but this performance is limited to ceramic or metal-can packaging as FET inputs are particularly sensitive to the induced stresses from plastic packages. In plastic packages the best devices offer 500µV - 1000µV of offset. Again Excalibur processing has reduced this V_{IO} shift in its TL051 and TL031 families of Bifets.

Matching FET gate-source voltages, V_{GS}, for low offset is more difficult than matching bipolar transistor base-emitter voltages. Bipolar transistors commonly have less than 20mV spread of V_{be} drops, but gate-source voltages of FETs may vary by several volts measured at the same current.

10.2 Input offset voltage drift

The major causes of offset drift with temperature are:

a) V_{GS} and V_P (pinch voltage) mismatch:

$$\frac{dV_{IO}}{dT} = (3.5\mu V/°C) \cdot (V_{P1} - V_{P2} - V_{IO})$$

A 1mV difference in V_P or a 1mV absolute offset voltage yield 3.5µV/°C drift, which is

comparable with similar bipolar sensitivity.

b) I_D mismatch:

$$\frac{dV_{IO}}{dT} = (1.1\mu V/°C) . \left(\frac{I_{D1}}{I_{D2}} - 1 \right)$$

A 1% drain current mismatch gives 11μV/°C drift. This shows that JFETs are 10 times more sensitive to current matching than bipolar input stages.

10.3 Input bias current

JFETs input bias currents are very low at 25°C but double for approximately every 10°C.

$$I_{IB}(T) = I_{IB}(T_o) . 2^{(T-T_o)/10}$$

If a very high working temperature is used the bias current can exceed that of a bipolar stage.

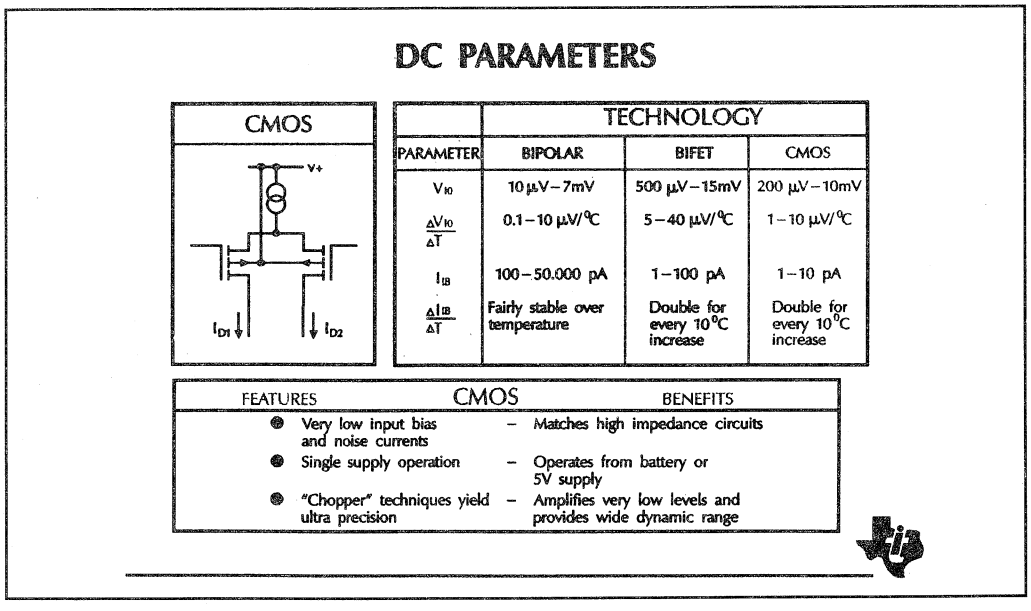


Figure11 - CMOS op amps

Standard MOS devices were renowned for having a very poor V_{IO} drift. However the phosphorous doped polysilicon gates used in TI's LinCMOS technology have enabled a family of devices with very low and stable offsets.

Silicon gate LinCMOS opamps provide similar features to JFETs but normally have lower and more stable offset voltages. The temperature sensitivity of LinCMOS input bias currents are similar to JFETS. This is due to a reverse biased diode in the ESD protection circuitry.

A special class of CMOS opamps use chopper stabilized techniques to yield excellent DC performance by continously re-calibrating themselves.

LinCMOS opamps have been optimised for single supply and low voltage operation.

OPAMP COMPARISON

Process	BIPOLAR	EXCALIBUR		BIFET	LinCMOS		
Device	uA741	TLE2021B	TLE2027A	TL051A	TLC2201A	TLC2652A	UNITS
V_{IO}	6000	100	25	800	200	1	µV
I_{IB}	500	50	35	0.2	0.005	0.01	nA
CMRR	70	100	117	75	90	120	dB
A_{VD}	86	120	140	94	104	135	dB
$\Delta V_{IO}/\Delta T$	(10)	(2)	1	25	(0.5)	0.03	µV/°C
$\Delta V_{IO}/\Delta t$		(0.006)	(0.006)	(0.04)	0.005	0.06	µV/mo

Worst case values @ 25°C. (xx) refer to typ value

Figure12 - Op Amp comparison

Comparing DC error parameter values for different technologies shows that modern bipolar opamps designed using new processes like Excalibur have a performance far exceeding that of industry standard bipolar opamps like µA741, LM301, LM324, etc. The offset, its drift and the input bias current have been greatly reduced while the open loop gain has been increased dramatically. TLE2021A has been designed for low power precision circuits and the TLE2027 for high precision circuits which still require low noise or high bandwidth. The Excalibur technology has improved the op amps offset stability with time over 100 fold when compared with similar competitive devices.

Bifet opamps normally have higher input offset voltage and drift compared to bipolar devices. The TL051 represents a second generation Bifet opamp with improved offset and stability over first generation products. Although the input bias currents of FET designs are insignificant when compared to their bipolar counterparts, over temperature their bias current doubles every ten degrees. Some bipolar designs actually have lower bias currents at higher temperatures.

Silicon gate CMOS technologies such as LinCMOS have reduced the problem of unstable offsets in MOS designs. The TLC2201, designed using LinCMOS, is an example of the new breed of CMOS devices. It offers extremly low and stable offsets while simultaneously featuring the high input impedance and low current noise found in the very best of JFET devices. For the ultimate in DC precision, chopper stabilised opamps such as the TLC2652, provides the absolute lowest input offset and drift. They are not expensive either.

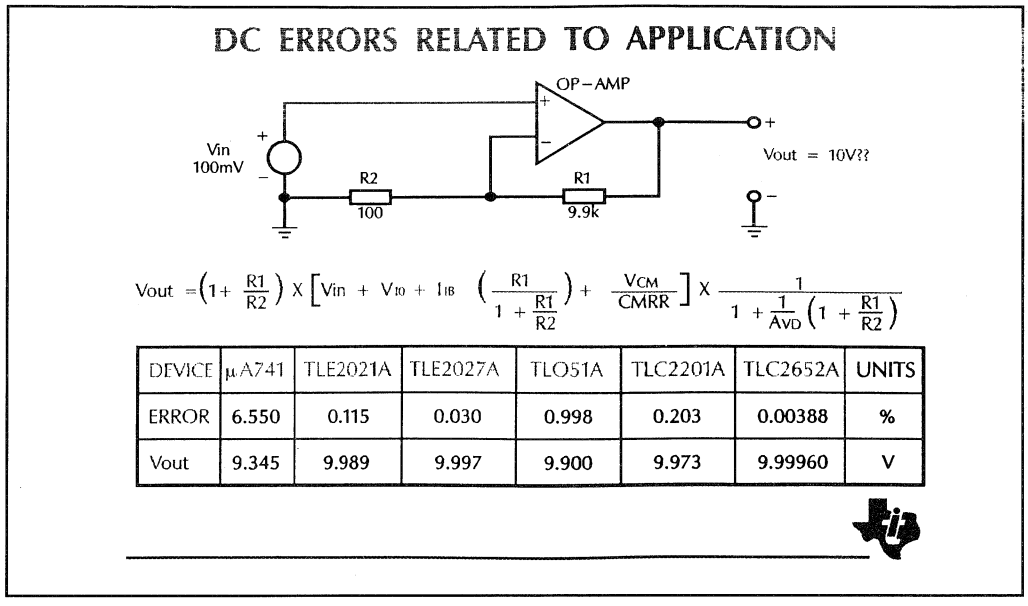


Figure 13 - DC errors related to application

Studying the errors in a simple non-inverting amplifier with gain of 100 demonstrates the importance of careful choice and use of op amps.

With 100mV input voltage, the expected output would be 10V. However, errors from input offset voltage, input bias current, finite common mode rejection ratio and open loop gain reduces the accuracy of the output voltage.

The error terms and the input signal are multiplied by the closed loop gain. If the circuit was an Inverting Amplifier the error and input signal would be multiplied by different gains. In inverting applications care must be taken as the closed loop gain can be larger than the signal gain with low gain circuits - this can cause significant errors due to the error signals.

Offset errors can be adjusted by external trimming. Using the adjust pins on single op amps to null an op amps offset can increase the temperature drift as the currents in the input stage are brought out of balance. This is more true for bipolar op amps than JFET or CMOS parts. The devices offset adjust pins should not be used to remove other system offsets.
Improved reliability and reduced trimming cost can be achieved by selecting op amps with initially low offset.

The input bias current creates a voltage drop across the parallel combination of R1 and R2 which is added to the offset voltage. When multiplied by the gain it appears that only the current through R1 contributes the output error. R1 should normally be choosen low such that the error voltage created is lower than the effect of the offset voltage. However, the opamp must of cause be able to drive the load impedance. This is often a problem in low gain applications. The TLE2021 has a maximum input bias current of 50nA at 25°C. With R1 = 2kΩ the bias current will contribute as much to the offset as the voltage offset. The error can be greatly reduced by inserting a resistor in series with the non-inverting input. By choosing its value to be R1//R2 the bias current error term is reduced to the input offset current

(difference in input bias currents of the inverting and non-inverting input) multiplied by R1.

JFET input or CMOS input op amp have very low input bias currents (picoamps) and can be used with even very high impedances without introducing significant errors (assuming the temperature range is moderate).

The input common mode voltage in this circuit is 100µV. Common mode voltages cause the offset to change with applied input voltage. The error term is expressed by the op amp's common mode rejection ratio. In the voltage follower mode with 10V DC applied to the input of TL051A which has a CMRR of 75dB, the offset may vary by up to 1.8mV. This is more than twice the specified voltage offset.

High open loop gain improves the accuracy of high closed loop gain applications. To correct for errors in resistor values a trimmer can be used to adjust the gain precisely. The open loop gain is however temperature, supply voltage and load dependant and hence its error contribution can not simply be compensated out with an adjustment.

The µA741 exhibits an 6.55% error in this circuit corresponding to only 3 bits of accuracy. The TLE2027A gives 11 bits and the TLC2652A 15 bits in this gain of 100 amplifier. The calculations are based upon worst case parameter values at 25°C.

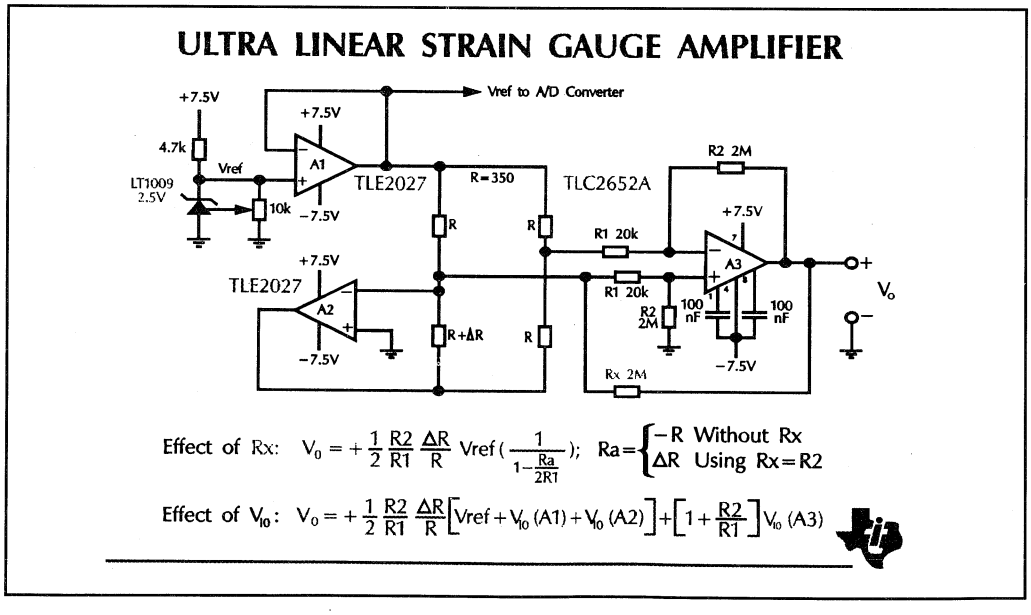


Figure 14 - Ultra linear strain gauge amplifier

To minimise errors in accuracy due to the self-heating of the strain guages the bridge is powered from a 5V supply. To reduce power consumption in the op amp's output stage the TLE2027s are powered from a +/- 7.5 Volt supply.

The excellent DC performance of the TLE2027 reduces errors from these opamps to insignificant values. By using a differential connection of A3, offset errors from A1 and A2 are

virtually eliminated. However, the offset error in A3 is multiplied directly with its configured gain.

To keep errors from bias currents low in the x100 amplifier, A3 is a chopper stabilized op amp (TLC2652A). This opamp features negligable bias currents due to its CMOS input structure in addition to an extremly low and stable offset.

The positive feedback resistor Rx provides an effective Z_{IN} of the A3 amplifier stage of more than 1MΩ eliminating loading effects of the bridge by the amplifier. Rx should be equal to R2. This resistor reduces the error from approximately 1% to an insignificant level if the variation in the bridge resistance δ R is small compared with R.

If the strain gauge used has all four legs active (two in compression and two in tension) or if just one side is active (one leg compressed and one under tension), then for optimum linearity the ground connection of the LT1009 band gap reference should be connected to the output of the op amp A2.

TLE2027 Features

Low Noise	... 2.5nV/$\sqrt{Hz}$ @ 1kHz
High Gain	... 45V/μV
Low Offsets	... 25μV max
Wide UGBW	... 15MHz typ

+ Output Saturation Recovery circuit

TLC2652 Features

Ultra Low Offsets	... 1μV max (TLC2652A)
	... 3μV max (TLC2652)
Low Drift/temp	... 30nV/°C max
Low Drift/time	... 20nV/month max
High Gain	... 135dB
Chopping Frequency	... 450Hz typ

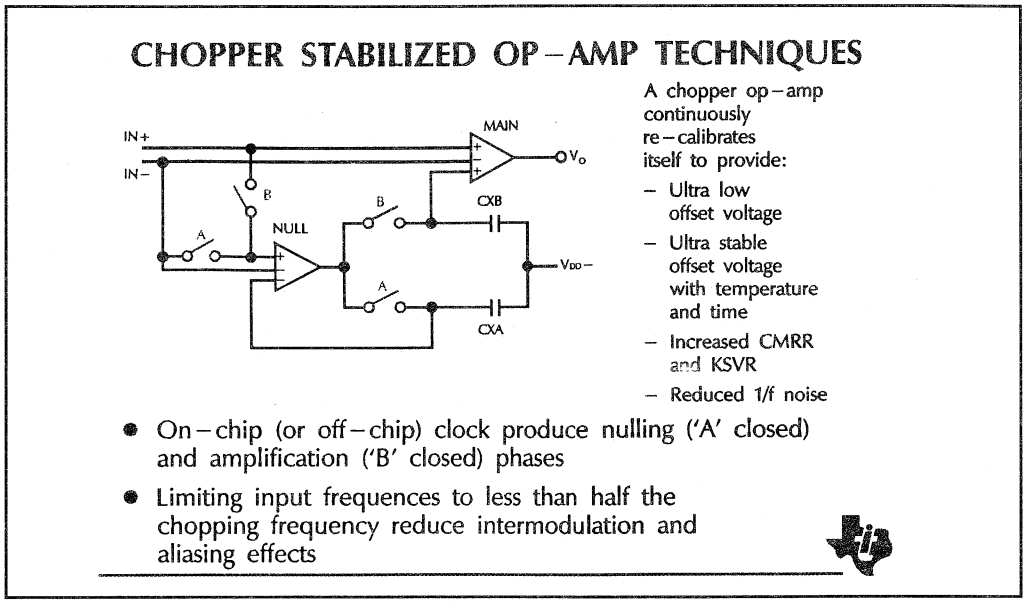


Figure 15 - Chopper stabilized techniques

Chopper stabilised op amps offer the best DC precision of any op amp. This superior performance is the result of using two op amps - a main amplifier and a nulling amplifier - and also an oscillator, switches and two external or internal capacitors to create a system that behaves as a single amplifier. With this approach, the TLC2652 opamp achieves sub-microvolt input offset voltage, sub-microvolt input noise voltage, and offset variations with temperature in the nV/°C range.

The on-chip control logic produces two dominant clock phases; a nulling phase and an amplifying phase. During the nulling phase, switch "A" is closed, shorting the nulling amplifier inputs together and allowing the nulling amplifier to reduce its own input offset voltage by feeding its output signal back to an inverting input node. Simultaneously, external capacitor CXA stores the nulling potential to allow the offset voltage of the amplifier to remain nulled during the amplifying phase.

During the amplifying phase, switch "B" is closed, connecting the output of the nulling amplifier to a non-inverting input of the main amplifier. In this configuration, the input offset voltage of the main amplifier is nulled. Also, external capacitor CXB stores the nulling potential to allow the offset of the main amplifier to remain nulled during the next phase.

This continuous chopping process allows offset voltage nulling during variations in time and temperature and over the common mode input voltage range and power supply range. In addition, because the low frequency signal path is through both the null and main amplifiers, extremely high gain is achieved.

The low frequency noise of the chopper depends on the magnitude of the component noise prior to chopping and the capability of the circuit to reduce this noise while chopping. The low frequency noise is reduced by increased chopping frequency. Intermodulation from input frequencies above the chopping frequency cause errors 60-80dB below full scale.

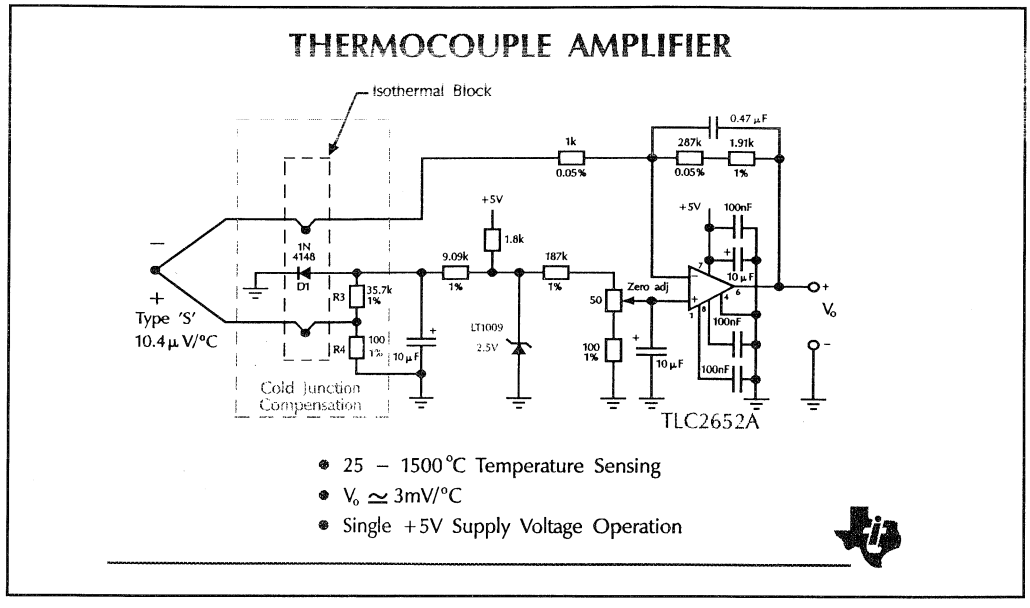


Figure 16 - Thermocouple amplifier

A thermocouple is a temperature sensor made from two dissimilar metals. When the junction is heated, a small thermo-electric voltage is produced which increases with temperature.

Thermocouples are low level devices. For an S-type thermocouple the output voltage average variation over its 0-1500°C temperature range is only 10.38μV/°C. Although linearity is poor, the temperature and voltage relationships are predictable and repeatable, so digital techniques can be used for linearization downstream.

Two thermocouple junctions are always present, a measurement junction and a reference junction. It can be proved that the temperature drift of the referance and measuremnt junctions are equal. It is therefore only neccessary to compensate for the drift with ambient temperature of the referance thermocouple - this technique is called 'cold junction compensation'. In this application the approximate -2mV/°C change of a low cost diode's forward voltage is resistively divided down to the thermocouple's sensitivity (6μV/°C) at 25°C ambient temperature. This counteracts any change in the reference junction temperature.

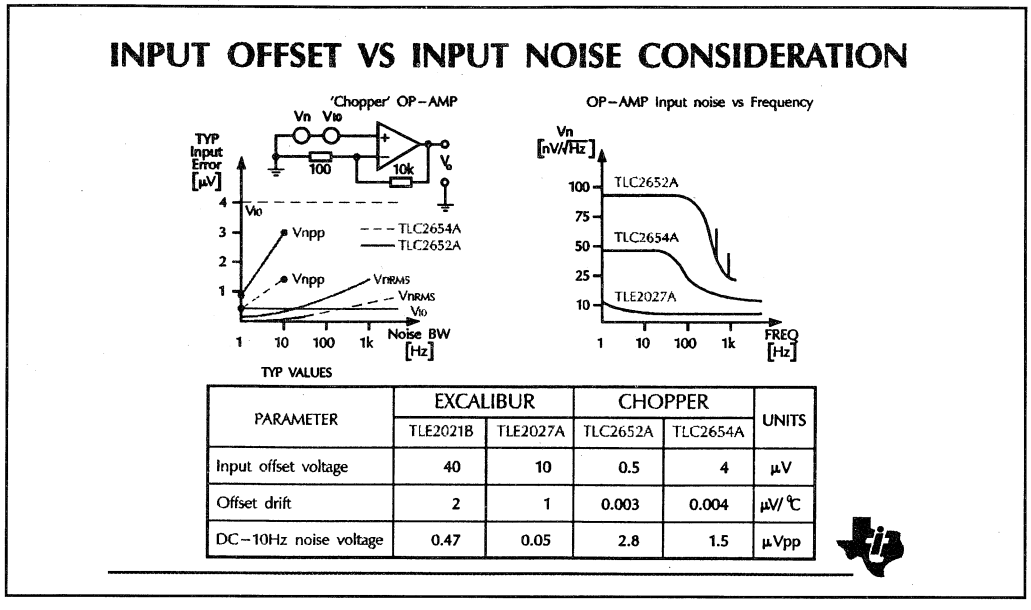
The circuit produces an output of 4.5V for full scale. As the circuit is operating from a single +5V supply, the opamp output cannot swing quite to GND thus limiting the lower end of the measuring range to 25°C. Ideally 0°C would produce 0V output voltage, V_o.

Accurate resistors can be avoided by introducing an additional gain setting trimmer.

Signal conditioning at such low levels is not a trivial matter. Careful choice of components, PCB layout, grounding and consideration of thermoelectric effects in all junctions areimportant. Noise should be limited from both reference and signal by appropriate filtering.

Because the signals are very small a high performance op amp with high open loop gain, low offset and drift is required. These care-abouts are best met by chopper stabilized opamps, such as the TLC2652A.

To take advantage of the extremely low offset voltage drift of the TLC2652A - 30nV/°C max - care must be taken to compensate for the thermo-electrical effects present when two dissimilar metals are brought into contact with each other. This includes device leads being soldered to a printed circuit board. Dissimilar metal junctions can produce thermo-electrical voltages in the range of several μV/°C which is several orders of magnitude greater than the chopper's offset drift. Air circulation and thermal gradients should also be prevented.



TYP VALUES

PARAMETER	EXCALIBUR		CHOPPER		UNITS
	TLE2021B	TLE2027A	TLC2652A	TLC2654A	
Input offset voltage	40	10	0.5	4	μV
Offset drift	2	1	0.003	0.004	μV/°C
DC–10Hz noise voltage	0.47	0.05	2.8	1.5	μVpp

Figure 17 - Input offset vs Noise consideration

When DC errors are as tiny as those achieved using a chopper stabilized op amps it becomes difficult to distinguish between the error sources. As chopper stabilized opamps are normally used in high gain configurations, the CMRR error can be ignored. If the supply voltage remains stable and at the level where the offset is specified in the datasheet the k_{SVR} (PSRR) error can also be ignored.

If the op amp operates over a bandwidth of say 10Hz the peak value of the low frequency noise often exceeds the ultra low offset voltage. Consequently, the offset becomes less important. If the offset voltage is cancelled out by adjustment, as in the case of the thermocouple amplifier application, noise becomes the dominating factor for the systems total accuracy. Unless the bandwidth is very limited the noise error far exceeds the temperature and time drift of the input offset voltage.

Bipolar Excalibur op amps offer low DC to 10Hz noise but are less stable than chopper stabilized amplifiers. This table indicates that, "choppers" are certainly the best choice where low drift is required and where it can be combined with low frequency noise averaging. The Excalibur devices (TLE2027), offer the best performance where a wide dynamic range is

required and DC errors including drift are less essential. However, in many instances a compromise proves useful.

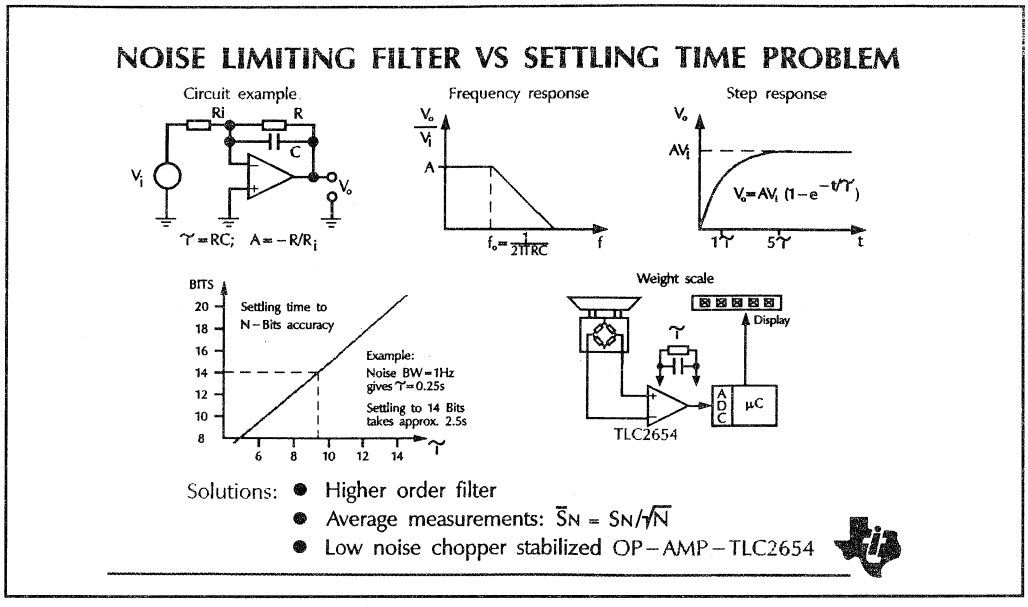


Figure 18 - Noise limiting filter vs Settling time

Noise reduction in a chopper stabilized application can be achieved by filtering the signal with a simple lowpass filter. However, when the bandwidth becomes limited the settling time from a step input to the final required accuracy becomes long due to the long time constant in the low pass filter. In applications such as thermometers where the temperature usually changes slowly due to the sensor's thermal time constant a very low cut off frequency can be used. In a weighscale application (such as those used at the checkout in a superstore) the sensor output changes very rapidly, and the settling time must be relatively short and comparable with the mechanical time constant to make the reading fast.

With f_o = 0.637Hz corresponding to a 1Hz noise bandwidth, the settling time to 14 bits takes approximately 2.5 seconds.

In such systems a compromise between dynamic range and settling time has to be made. The low noise chopper stabilized op amp TLC2654A optimises low noise while maintaining low and stable offset. The noise reduction compared with the TLC2652A is obtained by using a 20 times higher chopping frequency of 10kHz. This higher chopping frequency gives the device a usable bandwidth of 5kHz, without effects due to intermodulation between the input signals and chopping frequency.

TLC2654 features

Low Offset	... 10μV max (TLC2654A)
	... 20μV max (TLC2654)
Low Drift	... 0.05μV/°C max
	... 0.06μ V/month max
High Chopping Frequency	... 10kHz (5kHz useable bandwidth)

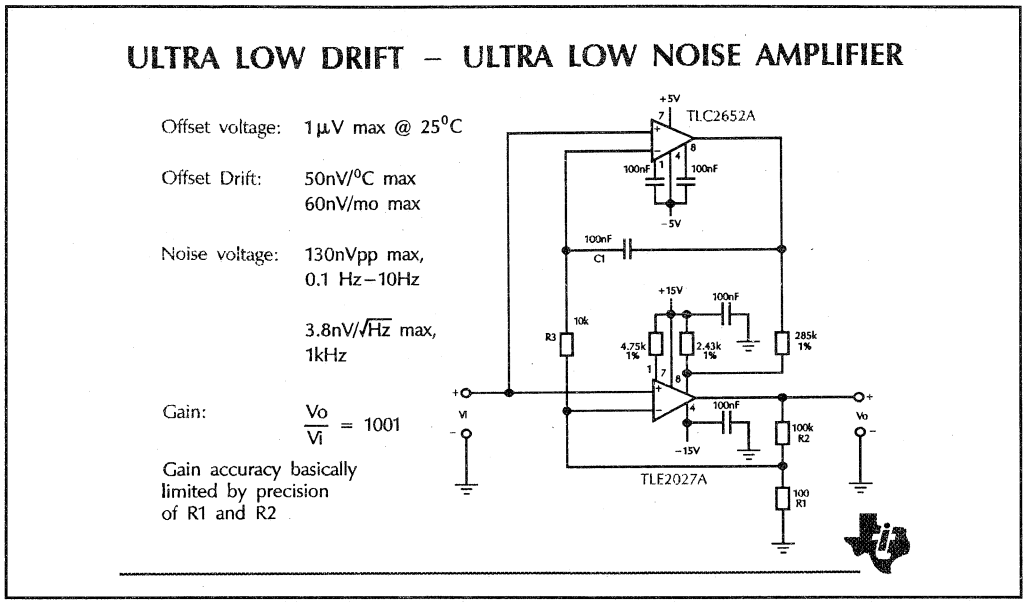


Figure19 - Ultra low drift - ultra low noise amplifier

Applications requiring extremely high DC precision combined with low noise can benefit from this composite amplifier.

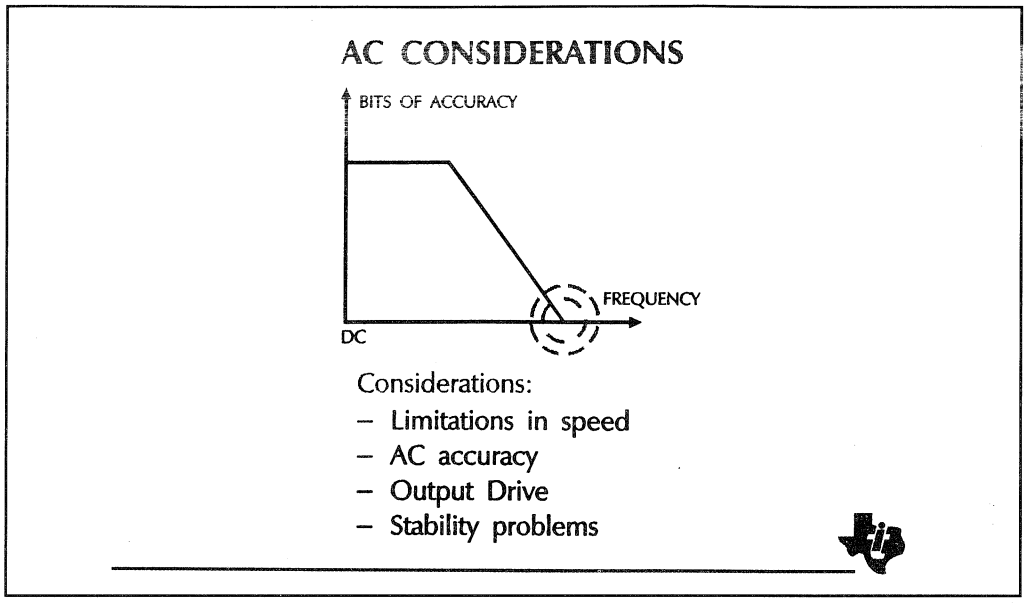
The TLC2652A measures the DC error at the TLE2027A's input terminals and biases its offset pins to force the offset to within 1µV. Similarly, the combined amplifier's offset drift with time and temperature is determined by the TLC2652A. The offset biasing at the TLE2027A is arranged such that the TLC2652A will always be able to find the servo point.

A 10 kΩ value for R3 minimises the error caused by TLC2652A's input bias current and its drift. The 100nF capacitor, C1, rolls off the TLC2652A at low frequencies ensuring that any AC signals do not affect the offset cancelation. The TLE2027A handles all AC frequency signals.

The noise of the composite amplifier is determined by the TLE2027A. Keeping R1 as low as 100Ω reduces its thermal noise and eliminates the affect of input bias current noise from the TLE2027A.

If the amplifier is used for high frequency applications, an additional RC filter network at the non-inverting input of the TLC2652A would prevent high frequency common mode signals from unbalancing its input stage, which could then cause changes in the offset voltage.

The settling time of the composite amplifier is affected by the DC correction loop and can limit its application for some high frequency circuits.



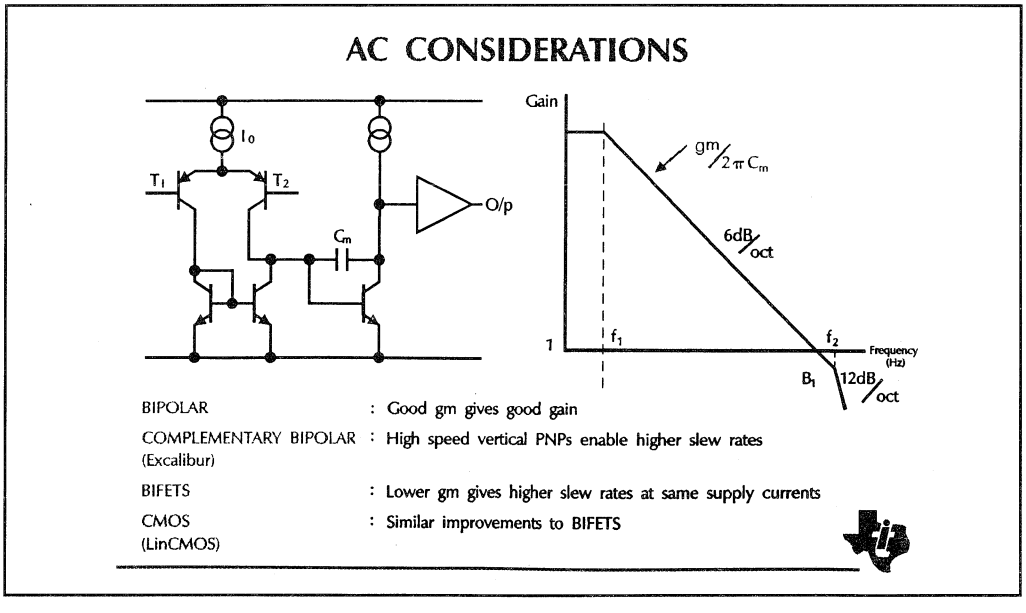


Figure 21 - AC considerations

Op amps require both AC and DC accuracy. Where parameters like V_{IO} and I_{IB} are relevent in DC applications other parameters should be considered in AC applications.

The basic structure of an op amp is split into 3 distinct stages; input with gain, level shift with gain and the output stage. Each stage causes phase shift. To ensure stability a Miller compensation capacitor is used. This capacitor limits the op amps slewrate and its gain at higher frequencies - ultimately defining the unity gain bandwidth. The AC performance of an op amp is determined by the process technology or the design techniques used. For instance,

the bandwidth of a device could be improved by increasing the supply current or by changing the technology.

Bipolar op amps were the first to be developed. These offer good gain and bandwidths but their slew rate for a given bandwidth is not very good. This is a limitation of the process (high transconductance, g_m) and is not something that can be easily designed out.

PNP transistors are normally used somewhere in the op amp design. Because they are usually much slower than their NPN counterparts they can severely affect an op amp's AC performance. Complementary bipolar technologies provide PNPs with f_Ts (transistor bandwidths) approaching that of NPNs - this enables much faster op amps to be designed without having to compromise parameters such as supply current.

Bifet op amps are designed with a combination of bipolar and JFET structures. P-channel JFETS (with much lower g_m's compared to bipolar transistors), are used in the input stage and the remaining circuit is designed with bipolar transistors. This combination has produced op amps with significantly higher slew rates for a given bandwidth than purely bipolar designs.

CMOS technologies, such as LinCMOS, have similar performance to Bifet designs, but are of particular benefit to low power or single supply applications.

The slew rate and bandwidth of an op amp are related. For example, the slew rate is approximately 0.32. B_1, for a single pole bipolar op amp. Devices with additional poles in their transfer function or processed with an alternative technology will have a different relationship.

AC PERFORMANCE : A COMPARISON

TECHNOLOGY	DEVICE	BANDWIDTH (MHz)	SLEWRATE (V/µs)	SUPPLY CURRENT PER AMP µA
BIPOLAR	µA741	1	0.9	1700
	LM324	0.6	0.2	250
EXCALIBUR	TLE2021	2	0.9	200
	TLE2027	15	1.7	3800
	TLE2061	2.1	3.4	280
BIFETS	TL051	3.1	18.0	2700
	TL031	1.1	2.9	200
LINCMOS	TLC272	1.7	2.9	1000
	TLC27M2	0.5	0.4	105
	TLC27L2	0.14	0.04	15

Values are typical

Figure 22 - Technology - Device comparison

The table above shows how the performance of a device is dependant upon technology and supply current. Old designs such as the LM324 using very basic IC technologies do not

compete with devices such as the TLE2021 which have been designed using a complementary bipolar process. The TLE2027 has multiple poles so although its bandwidth is high its slew rate is lower than would normally be expected. Bifets have high slew rates for a particular bandwidth without having particulary high supply currents, but unfortunately they have poorer and less stable offset voltages.

The TLC27X series of LinCMOS devices highlight how supply current affects AC performance. Each device is essentially the same, but the internal bias currents have been altered - each has a different supply current. Other parameters are also changed by this, such as the gain which is higher for the low bias version. Unlike Bifets, LinCMOS devices can operate from a single 5V supply.

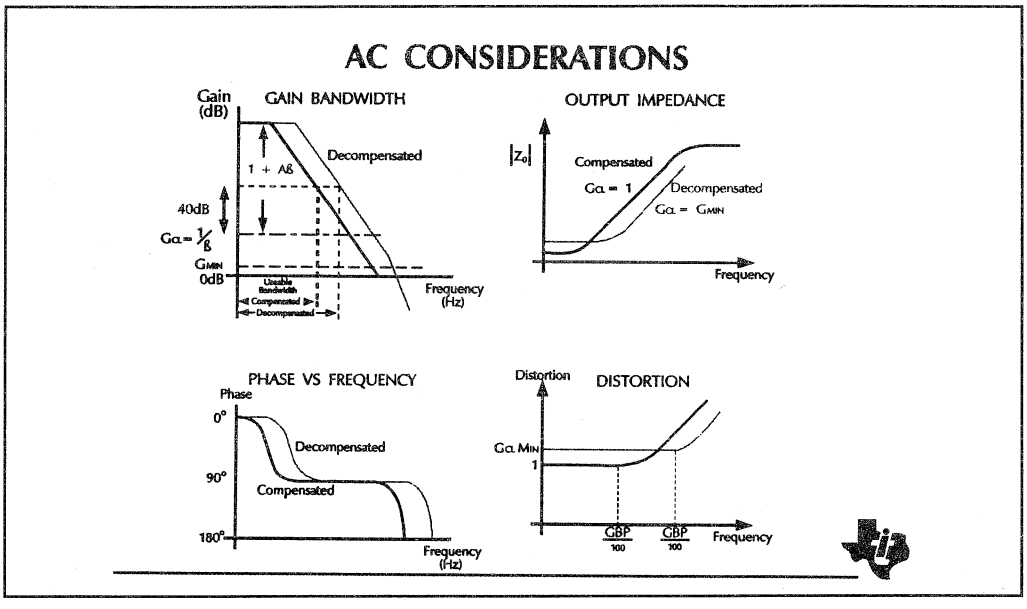


Figure 23 - AC design consideration

Op amps are designed to have wide gain-bandwidth product and large DC open loop gain. Normally negative feedback is used to 'desensitise' the system from variations in the open loop gain and to provide a system which is less sensitive to particular device parameters. The desensitising factor (1+Aß, where A is the open loop gain and ß is the feedback factor), provides extra stability, improves the accuracy of the output voltage, increases the input impedance and reduces the output impedance. It also reduces distortion and affects the CMRR and k_{SVR} (PSRR).

To ensure stability, the open loop gain is made to roll off at -20dB/decade. This places a limit on how fast you can operate the device before the desensitising factor starts to lose its effect.

So how fast an op amp is needed? The key problem is the falling off of the loop-gain, Aß. This is the amount of 'excess' gain which the negative feedback removes. A good design should normally allow for a loop gain of 20 - 40dB at the maximum frequency of interest. For

a gain of 10 at 10kHz the op amp should have a unity-gain bandwidth of 10MHz (assuming a single pole roll-off).

To enable designers to achieve higher gains at higher frequencies decompensated op amps are available. The Miller capacitor in these devices has been reduced to significantly increase their slewrate and bandwidth. These devices must operate with a gain higher than a specified minium (typically 5) otherwise the circuit will be unstable.

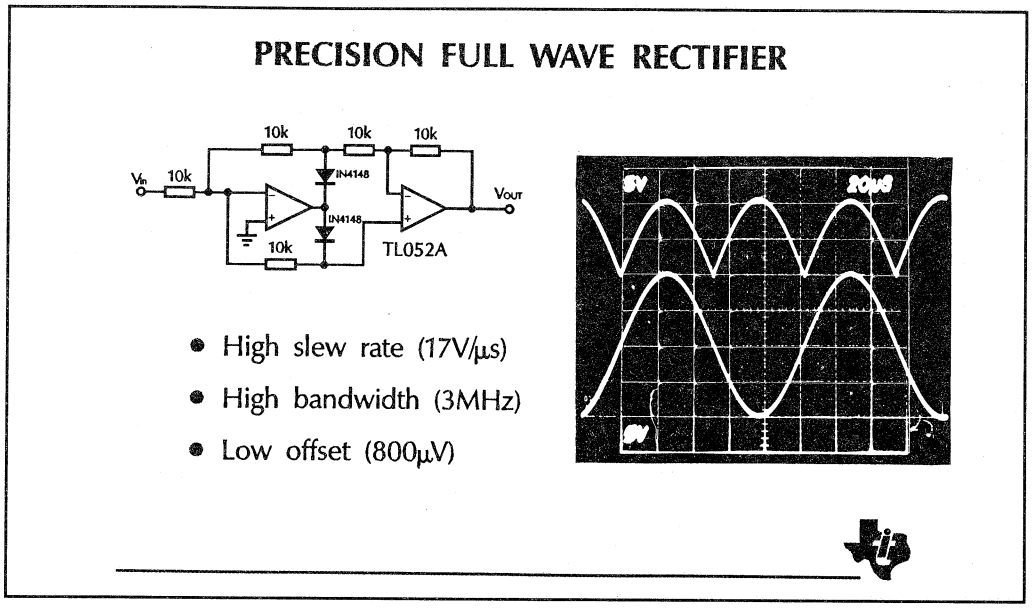


Figure 24 - Precision high speed absolute value circuit

Precision rectifiers are used in many applications. Op amps in these circuits require good AC performance, with high slewrates, wide bandwidths and also good DC precision.

To achieve the required AC performance Bifet op amps would normally be the first choice. Bifets however can suffer from poor offsets and bad drift and they may sometimes prove to be unsuitable in precision circuits. The TL052 devices, used in this application, were specifically designed to improve the DC perfromance of Bifets. Their AC performance has been slightly enhanced over industry standard products (TL071 family) but their DC precision is significantly improved.

The circuit shown here is a standard precision rectifier circuit. By using the TL052A it is possible to achieve high levels of accuracy and operation over a wide range of frequencies.

TL051 Features

Offset Voltage	... 800μV max
Offset Drift	... 25μV/°C max
	... 0.04μV/month typ
Slewrate	... 13V/μs min
Bandwidth	... 3MHz typ

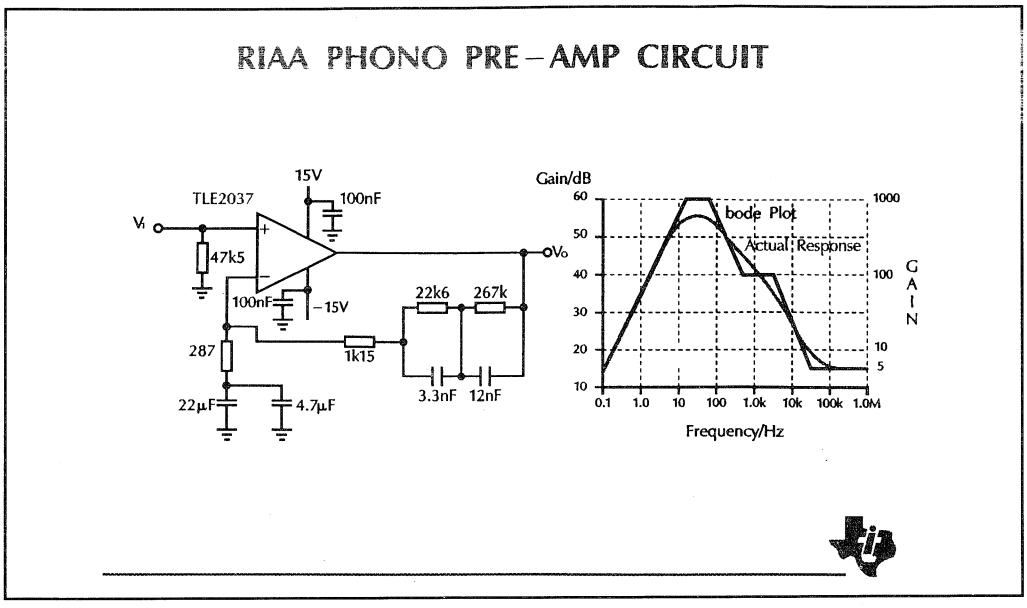


Figure 25 - RIAA high performance low distortion amplifier

A system requiring the ultimate in AC performance is audio hi-fi. CD players, with a dynamic range exceeding 90dB, are pushing the performance of amplifiers to new levels.

Phonographic recording/replay is still the standard for many good quality Hi-Fi and they require the ultimate in high performance amplifiers. The TLE2037 with an open-loop gain of 153dB, an offset of 25µV and a 80MHz gain-bandwidth product is an excellent choice in audio applications.

Record equalisation circuits illustrate the importance of high gain and wide bandwidth in an AC application.. The RIAA specification defines the characteristics of the phono replay pre-amplifier, and takes into account the frequency response of magnetic pick-ups. The pre-amp must match and cancel out the pick-up's response. The result is roll-offs at 50Hz and 2120Hz with a zero at 500Hz. The circuit incorporates a low frequency pole and a corresponding zero at 20Hz to remove rumble and low frequency record effects.

For a gain of 1000, the op amp needs a large gain-bandwidth product to remove any gain error. The chosen op amp, the TLE2037, has a loop-gain in excess of 40dB at 20kHz. As important, the device is still operating well within its full power bandwidth.

To achieve these levels of performance the op amp has been decompensated. This means that the compensation capacitance has been reduced to allow faster slewing rates and higher bandwidth. However the decompensated op amp will only remain stable for closed loop gains of greater than five. Therefore the high frequency gain of the circuit has been designed to flatten out with a gain of 5. This flattening occurs at 40kHz.

The types of components used must also be considered. The circuit has been purposely configured so as not to require the use of noisy, low performance electrolytic capacitors.

Polypropylene capacitors with their very low tan δ give good performance. For the lowest frequency zero a polycarbonate capacitor is been used.

The resistors used are all metal film for high precision and low flicker noise. They are readily available in E96 series values thus providing a cheap and accurate solution to the pre-amp's requirements.

TLE2037 Features

Offset Voltage	... 25μV max
Unity Gain Bandwidth	... 80MHz typ
Noise Voltage	... 2.5 nV/√ Hz
Large Signal Gain	... 45V/μV or 153dB typ
Distortion	... < 0.002%

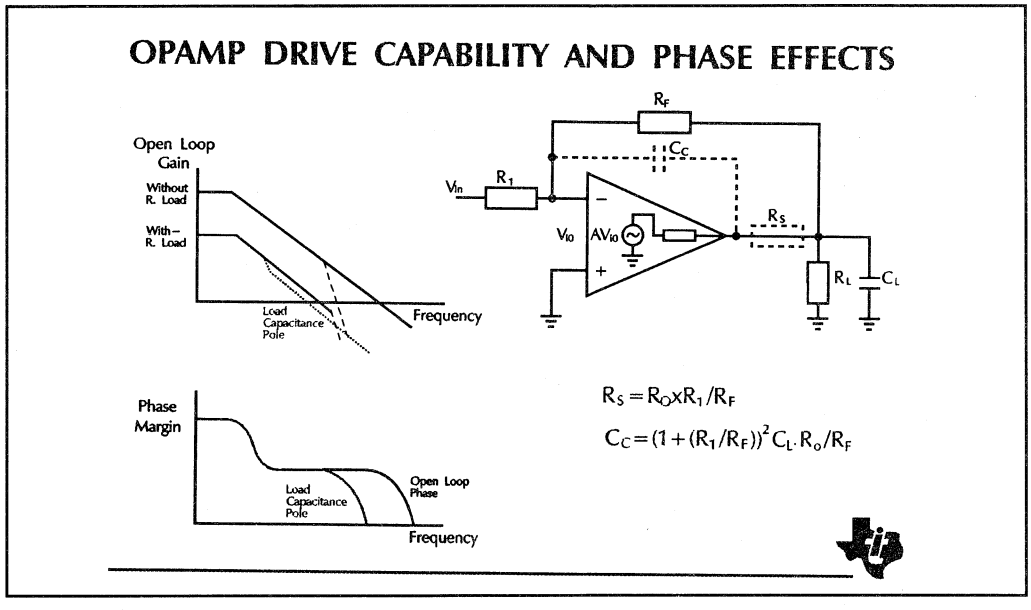


Figure 26 - Op Amp drive capability and phase effects

An operational amplifier's drive capability is important in many applications. The effect of the finite output impedance on both reactive (phase shifting) and resistive (power consuming) loads must be considered.

For resistive loads the output impedance will work with the load resistor to attenuate the open loop gain. This will affect the unity gain bandwidth and reduce the maximum output swing, therefore causing output distortion. Op amps with high loop-gains will reduce this effect at low frequencies.

For capacitive loads the output impedance will form a low-pass filter, which will ultimately introduce an extra 90° phase shift in the phase response of the amplifier. This will in turn cause degradation of the phase margin resulting in overshoot and settling time problems.

With resistive loads feedback reduces errors. With reactive loads feedback can increase them. Feedback reduces the open-loop gain to $A_{VD}/(1 + A_{VD}\beta)$. The extra pole created by the output impedance/load capacitance modifies the open loop gain, A_{VD}, by adding extra phase shift to its phase response. This can lead to oscillation.

To avoid this problem an op amp with a large phase margin should be chosen. An example, the TLE2061, has a Φ m=60° with a 100pF load.

Adding a resistor in series with the load capacitor, will also improve stability. If the resistor is placed outside the feedback loop (an increase in the output resistance which will not be reduced by the feedback), a 'zero' will be created which will reduce the pole's effect on the phase response of the amplifier. Alternatively, the extra resistor,R_S, can be kept within the feedback loop. This will reduce its effect on output impedance but will move the pole down to a lower frequency. To counteract this low frequency pole, an integrating capacitor, C_C, should be placed directly across the op amp. This latter method will unfortunately reduce the band-width of the circuit This effect can be minimised by choosing R_S and C_C using the formulae below;

$$R_S = R_O \cdot R_I / R_F$$

where R_I is the shunt resistance and R_F is the feedback resistance.

$$C_C = (1 + (R_I / R_F))^2 \cdot C_L \cdot R_O / R_F)$$

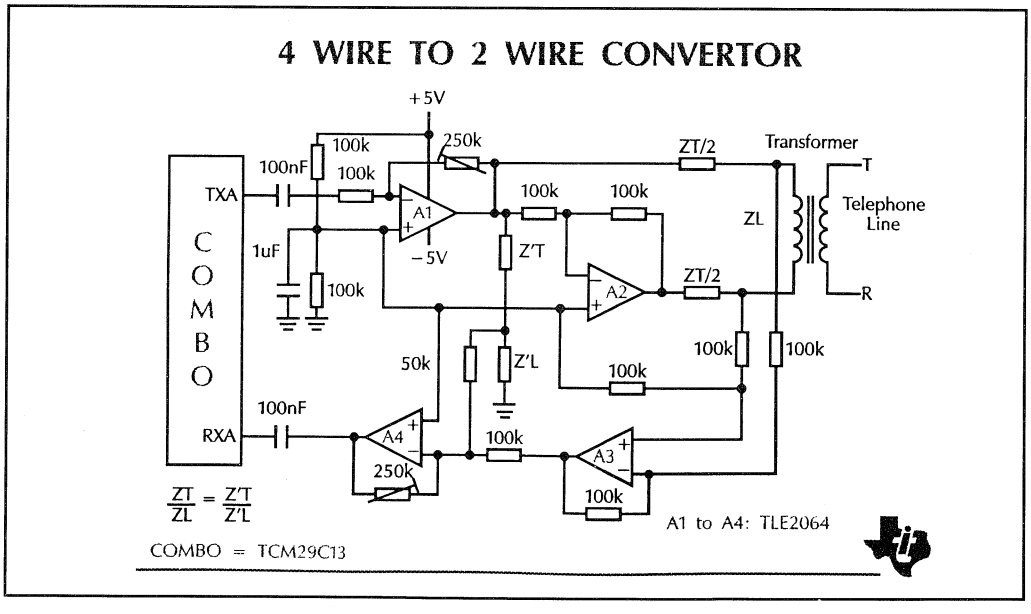


Figure 27 - Op Amp drive capability

This application shows the typical 2-wire to 4-wire circuit used in many telecom systems (eg. line cards and modems). Here the key op amp care-about is the requirement to drive the low impedance transformer effectively. Typically the transformer's impedance is 600Ω, but it can vary from 80Ω to 2000Ω. The op amp therefore requires good output drive, good stability and low distortion. Another important consideration for telecom circuits is power consumption.

Modems are often portable, linecards are power sensitive and the telephone companies are very restrictive on how much current they will provide down the line.

TLE2061 Features

Low Power	... 320µA max
Good Output Drive	... V_{OUT} = +/- 2.5V, with R_L=100Ω, V_{CC}=+/-5V
Slew Rate	... 2.5V/µs min
Power Bandwidth	... 140kHz

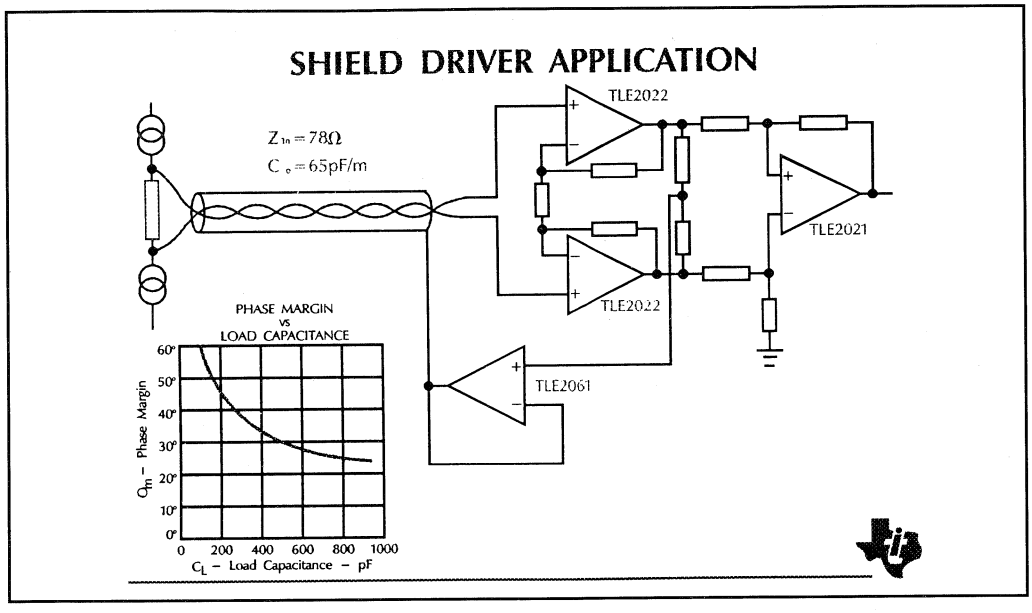


Figure 28 - Sensor cable shield driver

Remote sensors are common in many measurement systems. To reduce the effects of interfering signals and improve the signal to noise ratio the sensor cable will normally be shielded. The sensor then 'sees' this line as a large capacitive load. To reduce this effective capacitance, a shield driver circuit is usually implemented.

By driving the shield at the common-mode voltage of the signal running down it, the effective capacitance at the sensor's output is reduced. The signals at the instrumentaion amplifier's inputs are now much clearer.

The op amp driving the shield will see a large capacitive load. Because the device is configured as a unity gain amplifier, its phase margin and stability must be high. Trying to improve an op amp's phase margin by compensating with an external integrating capacitor would slow down the circuit and could increase the output impedance. The best solution is to use an op amp with a high phase margin. The TLE2060 family of Bifets have been specifically designed to drive low resistance and/or high capacitive loads.

The circuit above uses TLE202X in a standard differential amplifier configuration. The TLE2061 buffers the common-mode voltage along the shield.

TLE2061 Features

Supply Current	... 320µA max
Slew Rate	... 2.5V/µs min
Bandwidth	... 2MHz
Phase Margin	... 70° (R_L= 600Ω, C_L = 100pF)

TLE2024 Features

Supply current	... 280µA/amplifier
Low I_{CC} Drift	... <50µA over -55 to + 125 °C temp range.
Good Slew Rate	... 0.9V/µs
Good Bandwidth	... 2.8MHz

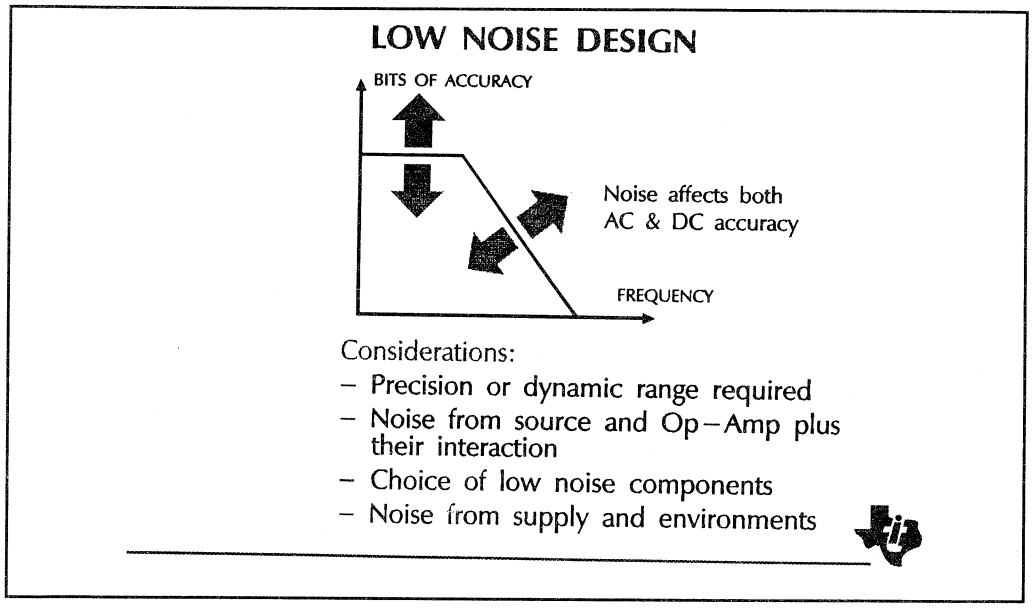


Figure 29 - Low noise design

Noise errors can degrade total system performance. In precision instrumentation design for example, the low frequency noise from DC to 1Hz or 10Hz is often essential and in audio design the wide band noise sets the limit for the dynamic range.

The source itself determines the lowest noise achieveable in any system. Added to the source noise is noise from the op amp. A part of this noise interacts with the source impedance and the external components used to implement the circuit.

Additional noise created by external components and the surrounding environment should also untilmately be considered. These noise sources can include: the power supply, ground, thermo-electric noise from moving air across thermo-electric junctions, electromagnetic or electrostatic induced hum, etc.

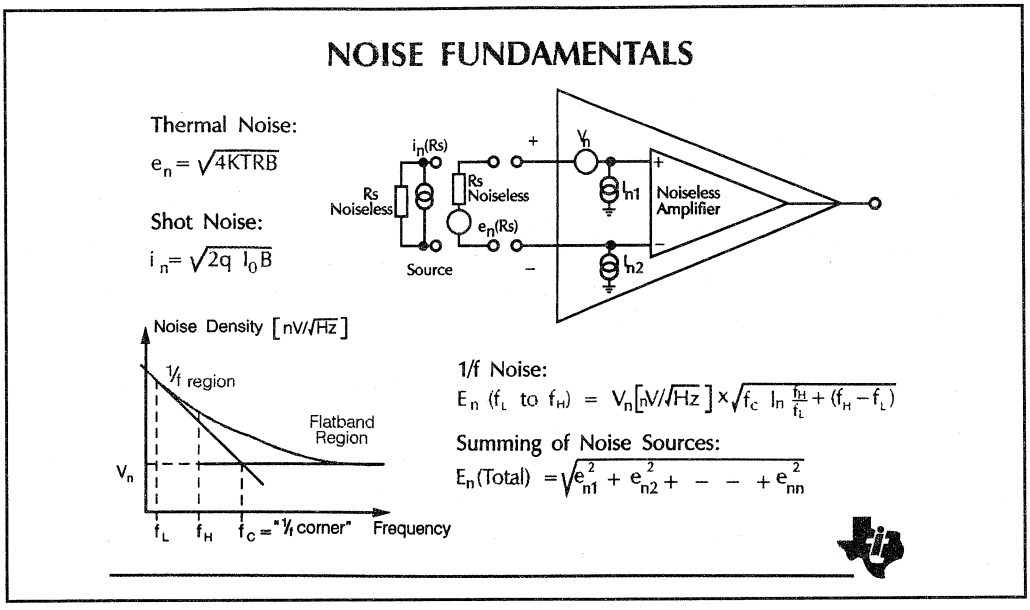


Figure 30 - Noise fundamentals

Noise in op amps and other electronic devices can be attributed to four main processes:

- o Thermal Noise
- o Shot Noise
- o Flicker Noise
- o Popcorn Noise

The noise discussed is related to the input of the op amp. The noise on the op amp's output will be input referred noise multiplied by the closed loop gain.

30.1 Thermal noise

Thermal or Junction noise is exhibited by all resistors due to the random motion of electrons in the resistive structure. The noise model for a resistor is a noiseless resistor in series with a voltage noise source:

$e(noise) = \sqrt{4KTRB}$ Volt;

or a noiseless resistor in parallel with a noise current source:

$i(noise) = (4KTB)/R$ Amps;

$K = 1.38*10^{-23}$ J/K; (Boltzmann's constant)
T = Absolute temperature in degrees Kelvin; (298 @ 25°C)
R = Resistor value in Ohms
B = Noise bandwidth in Hz

30.2 Flicker noise

The noise in the 1/f region can be calculated from:

$$e(1/f\ noise) = e(n) \cdot \sqrt{f_C \cdot \ln(f_H/f_L) + (f_H - f_L)} \quad \text{Volts}$$

f_C = Voltage noise "1/f corner frequency" in Hz
$e(n)$ = Spectral voltage noise density in flatband region in $V/\sqrt{Hz}$
f_H = Top of bandwidth of interest in Hz
f_L = Bottom of bandwidth of interest in Hz

The equation for the 1/f voltage noise also applies to 1/f current noise - the voltage parameters should be replaced by current parameters.

30.3 Shot noise

Shot noise is associated with current flow across a forward biased pn junction. A DC current is actually made up of discrete charges (electrons) being swept across the depletion region; consequently it exhibits a random noise pattern. The shot noise can be calculated from:

$$i(noise) = \sqrt{2 q I_o B} \quad \text{Amps}$$

q = 1.6×10^{-19} Coulombs; (electron charge)
I_o = DC operating current across pn junction in Amps (usually the input bias current for op amps)
B = Noise bandwidth in Hz

30.4 Popcorn noise

Popcorn noise sounds like popcorn popping when played through a speaker. It is characterized by "hopping" between discrete noise levels. These can last from milliseconds to seconds. The source is not clearly understood but is reduced by cleaner processing. Good low noise processes should have no popcorn noise.

30.5 Combining noise sources

Noise generated in op amps and passive components as a result of physical processes is unpredictable. The noise is random, mostly Gaussian and is usually characterised as a root mean square value. The most widely used characteristic is the root mean square (RMS) value. As noise sources usually can be regarded as uncorrelated they can be summed as RMS values.

$$e(noise\ total) = \sqrt{e_1^2 + e_2^2 + - - + e_n^2}$$

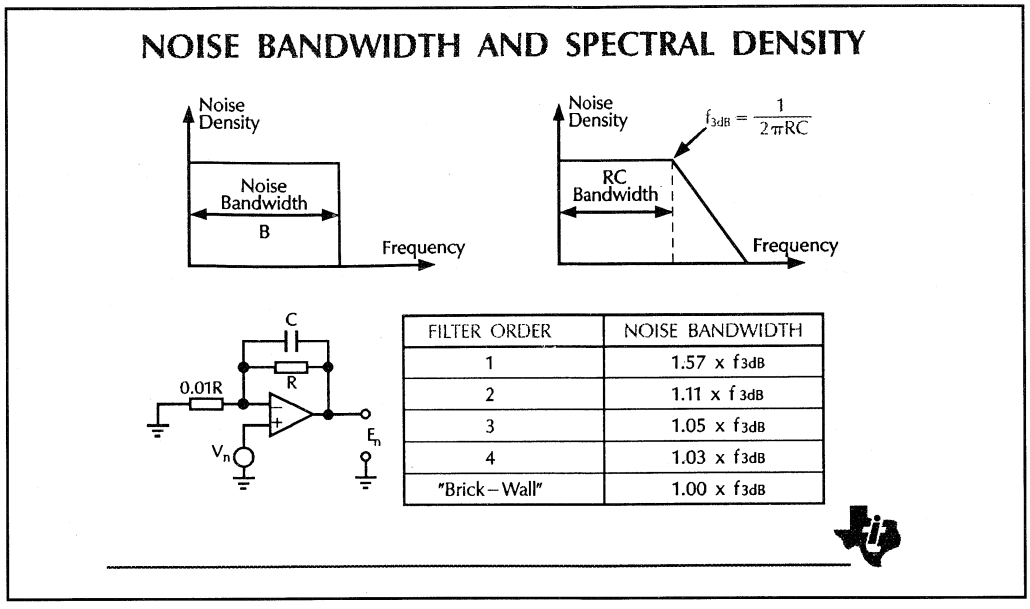


Figure 31 - Noise bandwidth and spectral density

The noise bandwidth, B is not the same as a common RC filter's 3dB bandwidth. Instead, noise bandwidth has a "brick-wall" filter response. The maximum power gain of the a transfer function T(jw) multiplied by the noise bandwidth must equal the total noise which passes through the transfer function. Since the transfer function power gain is related to the square of its voltage gain we have:

$$T_{MAX}^2 \bullet B = \int_0^\infty |T(jw)|^2 \, dw;$$

Where, T_{MAX} = Maximum value of T(jw)
T(jw) = Transfer function voltage gain
B = Noise bandwidth in Hz

For a single RC roll-off, the noise bandwidth B is:

$B = (\pi/2) \cdot f(3dB \text{ for RC filter});$

For higher order, maximally flat filters, see table above.

If a low pass filter, with a single pole, has a $f(3dB) = 1/(2\pi RC) = 20kHz$, then the noise bandwidth would be 31.4kHz.

If you measure the noise from 0.1Hz to 10Hz, which is especially relevant in low frequency instrumentation design, you must also consider the measuring equipment's performance at these low frequencies.

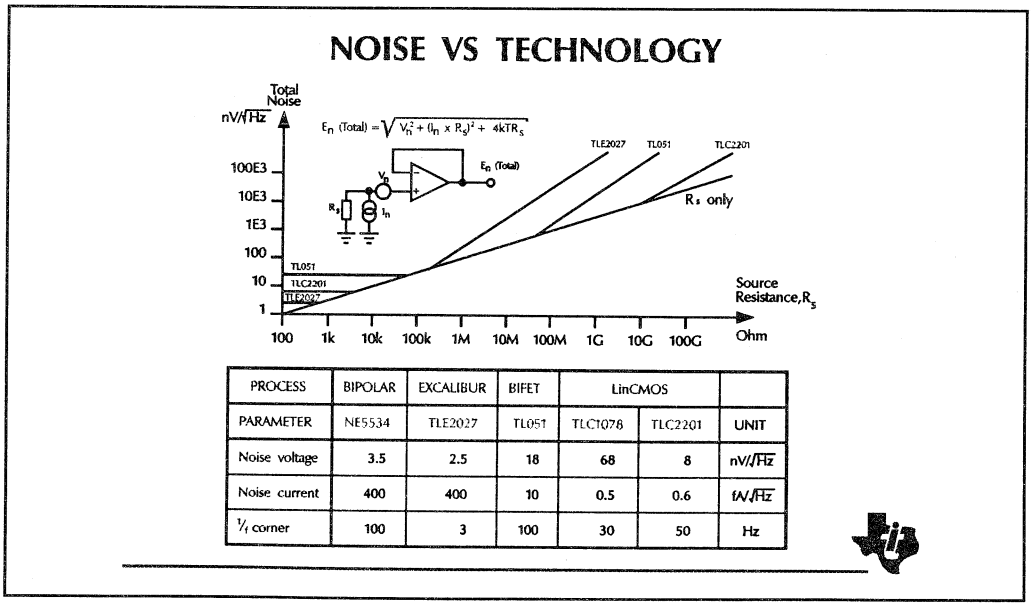
The total noise in a circuit is specified in volts. However, often it is convenient to compare and operate with noise terms using the spectral density. This is the noise per squareroot Hertz usually specified in datasheets as:

$$nV/\sqrt{Hz}.$$

To change from RMS voltage noise to peak-to-peak voltage noise (in the flatband), multiply by 6.6. This gives you 99.73% certainty your peak-to-peak noise will not exceed this value. The statistical certainty factor is an important consideration for the total error in systems where the analogue signal is sampled or measured by a peak detector. For 99.99% certainty you must multiply the RMS value by 7.8 to obtain the peak-to-peak noise.

In wideband applications such as audio the RMS value of the "white noise" or flatband noise is much more important than the low frequency noise, - the human ear is much less sensitive to low frequencies than to midband frequencies. The sensitivity to 20Hz is approximately 50dB lower that the sensitivity to 1kHz.

In instrumentation design where a DC voltage is measured, the noise band is normally limited to a few Hz. However, very low frequency peak-to-peak voltage noise from the amplifier directly adds to or subtracts from the measured voltage from the sensor. In such systems the peak-to-peak noise is more relevant than the RMS.



PROCESS	BIPOLAR	EXCALIBUR	BIFET	LinCMOS		
PARAMETER	NE5534	TLE2027	TL051	TLC1078	TLC2201	UNIT
Noise voltage	3.5	2.5	18	68	8	$nV/\sqrt{Hz}$
Noise current	400	400	10	0.5	0.6	$fA/\sqrt{Hz}$
$1/f$ corner	100	3	100	30	50	Hz

Figure 32 - Noise vs Technology

Bipolar op amps offer the lowest voltage noise among commercialy available opamps. The voltage noise from a bipolar input stage in the flatband is dominated by thermal noise from the base spread resistance and the emitter small signal resistance. TLE2027 or the decompensated TLE2037 represents such op amps optimised for low voltage noise.

The current noise is basically the shot noise coming from the input's bias current.

Bipolar input op amps are best for low noise voltage. However, the current flowing through the input stage gives a bipolar op amp significant input bias currents. This implies relatively high input current noise. To reduce the bias current and therefore the current noise superbeta input stages or bias current cancellation circuits are used.

FET input op amps have an input noise current given by the shot noise from the gate current. This is very low at temperatures around 25°C compared to the base current in bipolar inputs. Consequently, FET input opamps have negligible current noise and provide superior noise performance with high impedance sources.

A FET input stage will have higher voltage noise and also a higher 1/f corner frequency than bipolar.

The noise sources of a MOSFET input device are similar to those of the junction FET. The gate current is negligible and the input current is reduced to leakage currents in the ESD input protection network.

A disadvantage of MOSFETs, in general, is their relatively high voltage noise and high 1/f frequency. However, an exception is the Advanced LinCMOS TLC2201 opamp. This offers a current noise level similar to the very best FET input op amps and a voltage noise comparable to many bipolar designs. In addition, an offset of only 200μV max, coupled with a very low drift over time and temperature, plastic package, operation from a single 5V supply plus rail-to-rail output swing make this device superior in its class.

Summarising:

Bipolar input stages give the lowest voltage noise and lowest 1/f corner frequency and are well suited for interface to low impedance sources. JFET and CMOS input stages have negigible input current noise allowing them to be used with extremely high source impedances. Noise current is related to the input bias current it will increase by $\sqrt{2}$ for every 10°C temperature rise.

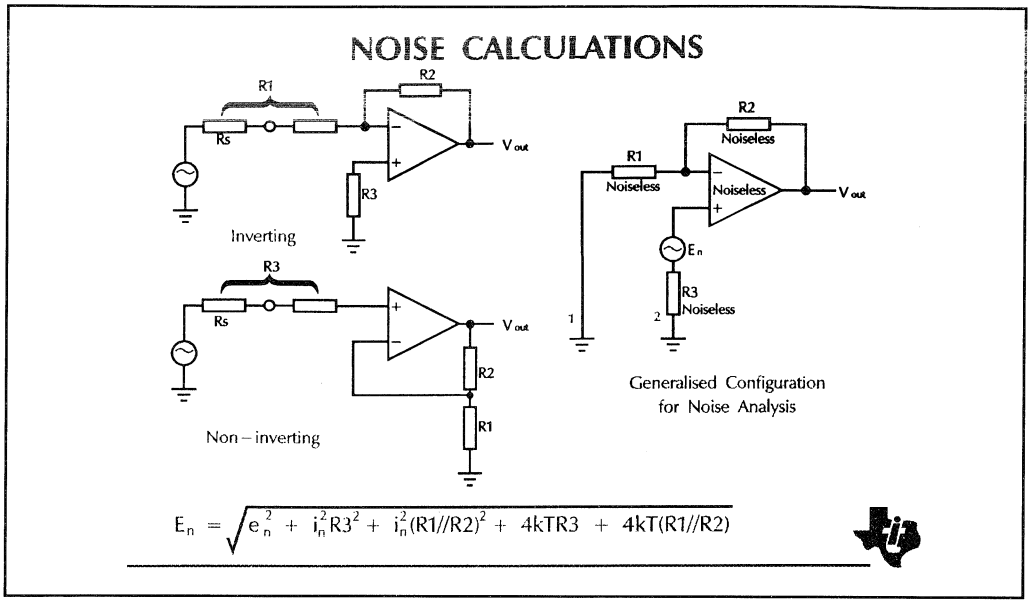


Figure 33 - Practical noise calculations

The circuit topology for the noise analysis of inverting amplifiers is identical to that for non-inverting amplifiers.

The effects of thermal noise in the resistances and the noise voltages developed across the resistances due to the bias current noise must be combined with the intrinsic voltage noise of the op amp. The impedance seen at the non-inverting input is simply R3, while the impedance at the inverting input is R1 in parallel with R2. From this the equation for the equivalent noise at the op amp's inputs (E_n) can be determined by inspection. From this equation, the noise referred to the signal input and the noise at the output can be easily calculated.

33.1 Inverting Case

The signal is applied to node 1 and node 2 is left grounded. The noise at the output is $(1+R2/R1).E_n$. This value is divided by the signal gain (R2/R1) to give the noise referred to the signal input which is $(1+R1/R2).E_n$.

For low noise applications where DC precision is not important (eg. audio), the bias current compensation resistor (R3) should be made zero. Removing the bias compensation resistor removes both its thermal noise, and the noise due to the noise current flowing through it.

33.2 Non-Inverting Case

Node 2 becomes the input and node 1 remains grounded. The noise at the output is clearly the same as for the inverting case (it is the same circuit). However the noise referred to the signal input is E_n. This is clearly better than for the inverting circuit, although this advantage diminishes with higher gains.

R3 includes both the source resistance and any bias compensation resistor. Again, if low noise is more important than DC precision, the bias compensation resitor should be removed. This reduces the value of R3 down to the source resistance (Rs) of the input signal thus reducing the noise.

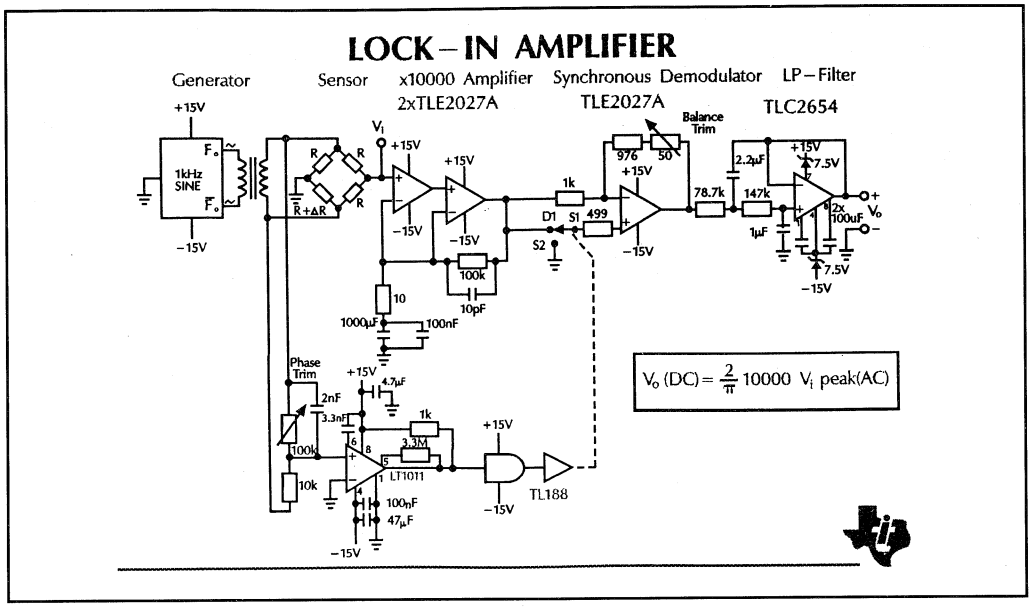


Figure 34 - Lock in amplifier

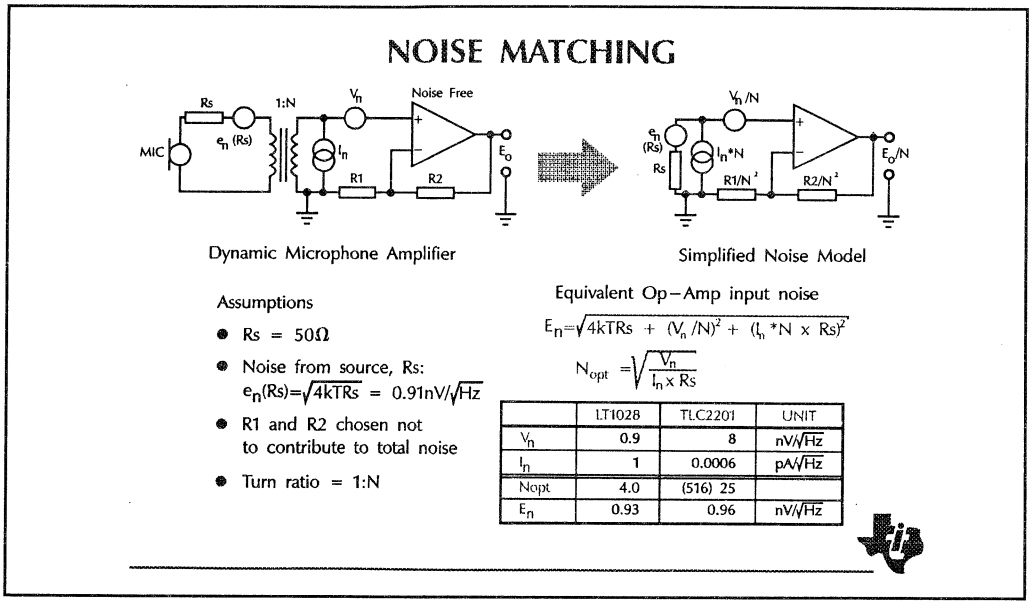
Feeding a sensor bridge with an AC signal rather than a DC signal allows outputs from capacitive, inductive as well as resistive sensors to be measured. Additionally, the sensitivity can be very high and is usually only limited by the thermal noise of the sensor, the noise of the high gain sensor amplifier and the systems bandwidth. When the signal frequency is constant a very narrow bandpass filter following the high gain amplifier can extract sensor signals burried in noise. A further signal rectification and averaging gives a DC output proportional to the sensor change. However, to build a narrow bandpass filter with, for instance, a 1kHz center frequency and a 1Hz bandwidth requires very precise components to ensure frequency accuracy and stability. Similarly, the sine generator frequency must be very accurate and stable.

This application shows one way to get over the frequency accuracy problem. The principle is still based on an AC carrier approach converting a change in a sensor impedance to a DC voltage. The amplifier shown is followed by a synchronous demodulator that detects the amplified carrier modulated sensor signal. Because the desired signal information is contained within a carrier, the system constitutes an extremely narrow-band signal path. Non-carrier related components are rejected and the amplifier passes only signals which are coherent with the carrier.

The very high gain (x10000) AC amplifier is implemented by using a double TLE2027 amplifier block to achieve an impressive 160dB open loop gain at 1kHz. The composite amplifier provides a typical 3dB bandwidth of 150kHz with a very accurate closed loop gain of 10000.

The zero transition synchronized demodulator implemented by another TLE2027 shift its gain between +1 and -1 in phase with the 1 kHz carrier. The "rectified" output signal is then smoothed with a 1Hz active filter around the TLC2654 to provide a DC output, V_O, proportional to the sensor bridge output, V_S.

The dynamic range of the circuit is from $1\mu V_{pp}$ to $1mV_{pp}$ at V_S. With $20V_{pp}$ across the bridge, the δ R/R sensitivity of the system is able to measure a change in the sensor from one part in a million fairly accurately.



Foil 35 - Input impedance matching

Source matching techniques can improve the noise performance of a circuit.

Low impedance dynamic microphones usually have a differential output. A differential cable to the amplifier and a good common mode rejection ratio in the amplifier prevent noise and hum pick-up from interfering with the signal. Two configurations are possible to convert the differential signal to a single ended signal; a differential amplifier or a transformer coupling.

A single op amp differential amplifier will be more noisy than the source impedance itself due to thermal noise from the input resistors. A high input impedance two or three op amp configuration instrumentation amplifier is an alternative but a transformer is often used.

The transformer converts the differential signal to a single ended signal. Secondly, it steps-up the signal (and therefore the microphones noise) to a level whereby the op amp haves a less dominant affect. However, the disadvantage is that a transformer with a turns ratio 1:N not only steps up the signal and noise voltage by N but it also increases the amplifiers source impedance by N squared. The result is the current noise of the op amp now needs to be considered.

The LT1028, available from TI, is the worlds lowest voltage noise commercial op amp available today. Its has only 0.9nV/($\sqrt{Hz}$) typical noise and is suitable for interfacing to low source impedances. The current noise of 1pA/($\sqrt{Hz}$) is however high compared with the 0.6fA/$\sqrt{Hz}$ current noise of the LinCMOS op amp TLC2201. However as shown, the total noise using the TLC2201 can be optimized, by noise matching, to be very similar to the noise of the source impedance. A higher turns ratio will further optimize the circuit but may prove unrealistic in practise.

TLE2027 Features

Noise Voltage	... 2.5nV/$\sqrt{Hz}$ @ 1kHz
Unity Gain Bandwidth	... 15MHz typ
Offset Voltage	... 25μV
Open Loop Gain	... 45V/μV

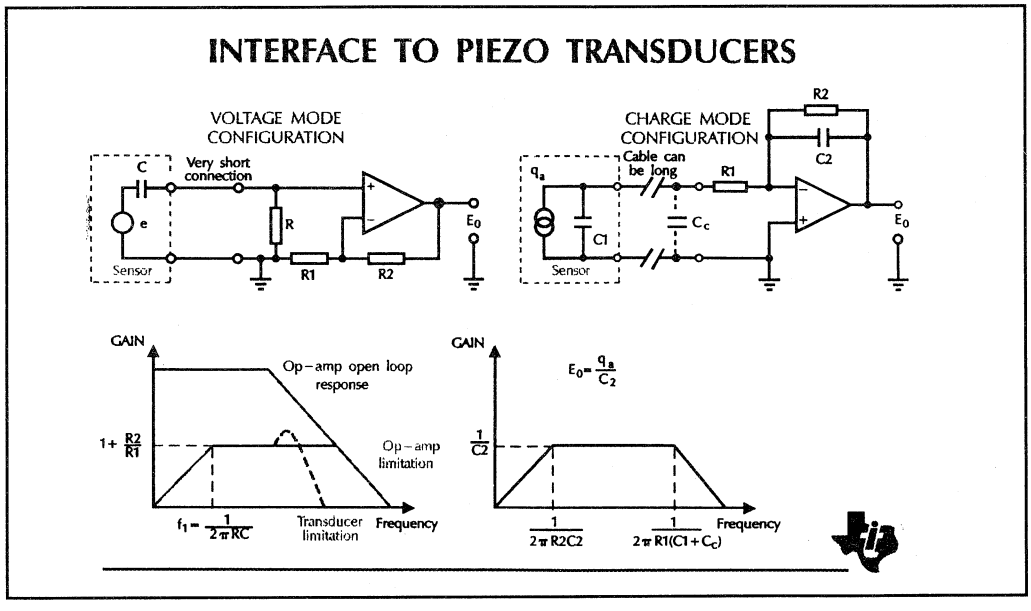


Figure 36 - Interface to high impedance sources

Op amps that interface to high impedance sources like piezo-electric transducers can be configured in two basic modes of operation: Voltage mode or Charge mode. Both principles require an op amp with very high input impedance and low bias current.

Voltage mode operation requires that the op amp is placed very close to the sensor as parasitic load capacitance on the sensor output will change its sensitivity. The sensors output signal is divided between the transducer's capacitance and any external parasitic load capacitance across the resistor R. A flat frequency response is limited by R and C plus the transducer or amplifier's upper frequency response. The voltage source "e" represent the product of the voltage sensitivity, S_V and the applied mechanical parameter.

Charge mode operation is widely used, primarly because the influence of the shunt cabel capacitance, C_C, across the sensor circuit is eliminated. Consequently, the length of a connected cable will not influence the sensitivity but only affect the maximum bandwidth of the measur-

ing system. The basic transfer function is $E_o = q_a/C_f$, where q_a is the product of the charge sensitivity S_q and the applied mechanical parameter. The op amp requires a DC current path for each input's bias current to flow; hence it is necessary to insert the resistor R_f in the feedback loop. In the absense of this resistor, the capacitors will build up a DC charge until the output reaches saturation. This resistor limits the lower cutoff frequency of the charge amplifier. For stabilisation purposes and for protection of the amplifier's input stage, the resistor R1 is inserted. This resistor also limits the upper frequency response. Without R1 the upper frequency limit is determined by the open loop characteristics of the op amp or by the transducer's resonant frequency.

For both the voltage and charge configurations a FET input op amp is usually the first choice but recent developments in CMOS design has yielded the Advanced LinCMOS TLC2201 challenging the FET input op amps on both noise and DC performance.

TLC2201 Features

Voltage Noise	... 8nV/$\sqrt{Hz}$ @ 10Hz
	... 18nV/$\sqrt{Hz}$ @ 1kHz
Current Noise	... 0.6fA/$\sqrt{Hz}$
Offset Voltage	... 200µV max
Single or Dual Supply	... Characterised @ 5V & +/- 5V

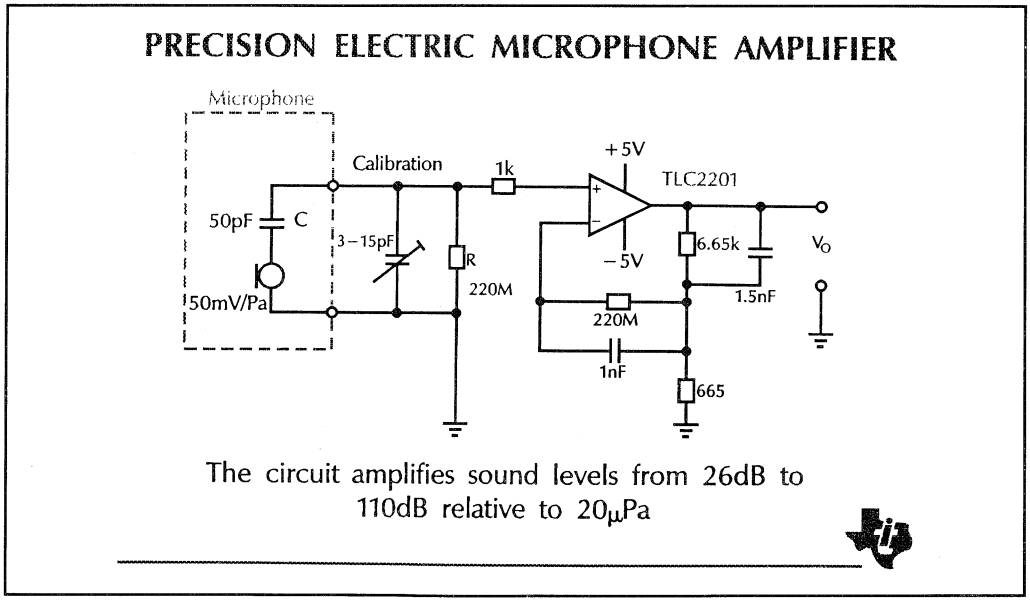


Figure 37 - Piezo microphone interface

The sensor used is a precharged piezo type condensor microphone (B&K type 4155), which exhibits approximately 50mV/Pa sound pressure level. The capacitor microphone can be modelled by a voltage generator in series with a 50pF capacitor. An adjustable capacitive signal divider provides a simple solution for trimming the sensitivity.

The sensor capacitance C and the load resistor R form a high pass filter at 15Hz. R2 and C2 give a roll off at 16kHz before the microphone and op amp roll off themselves. The 1kΩ resistor in series with the non-inverting input protects the op amp input by limiting the current if the microphone is not connected.

The total noise of the circuit, referred to the input, is typically 10mV or approximately 20dB relative to 20mPa sound pressure level.

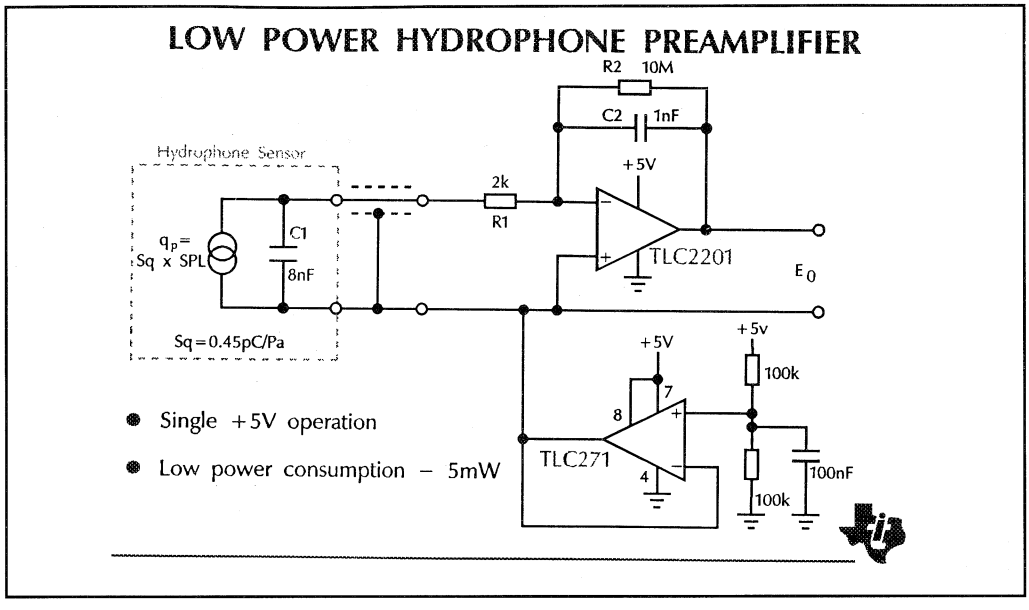


Figure 38 - Low power hydrophone amplifier

This charge coupled hydrophone circuit operates from a single +5V supply. The TLC271, configured in the low bias mode, forms a low impedance floating ground potential for the TLC2201 at +2.5V. The total power consumption is only 5mW for this low noise circuit.

The hydrophone (B&K Type 8105) exhibits 0.45pC/Pa sound pressure level. The sensor can be modelled by a charge source in parallel with a 8nF shunt capacitor. The lower frequency band is limited by R1 and C1 to 16Hz. Rf and Cf provide a high frequency roll-off at 16kHz.

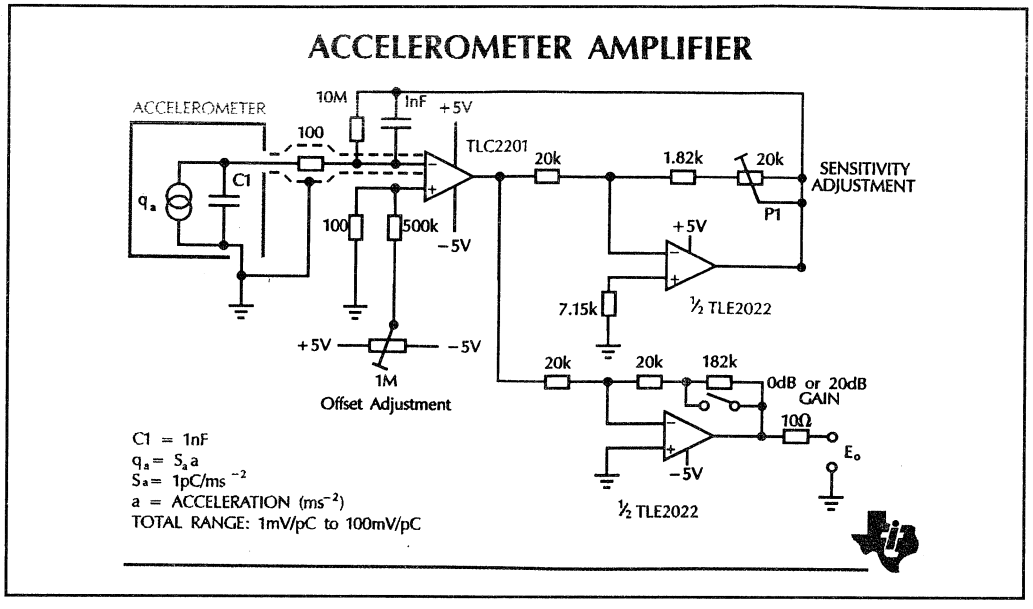
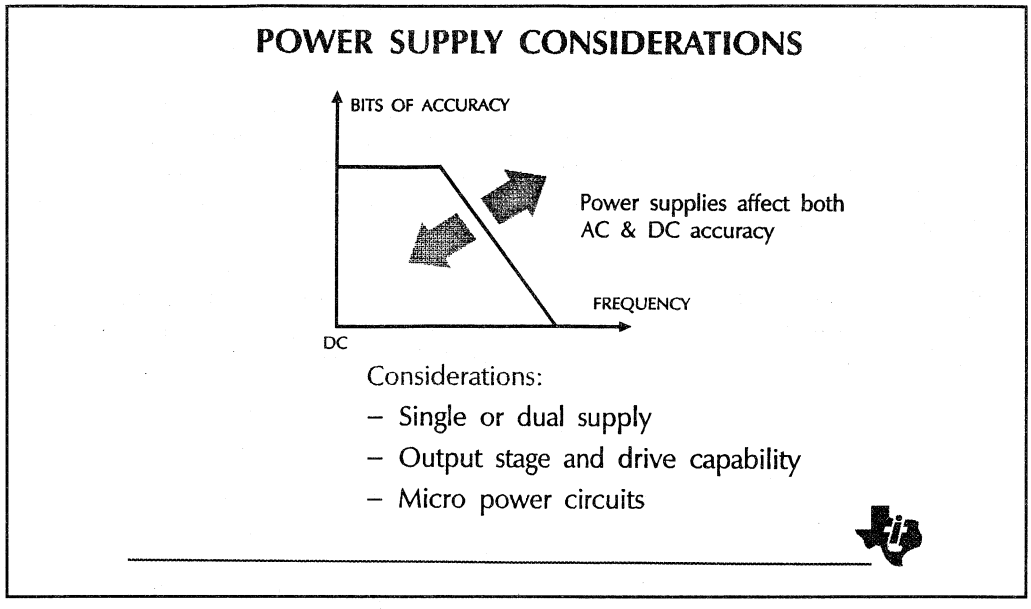


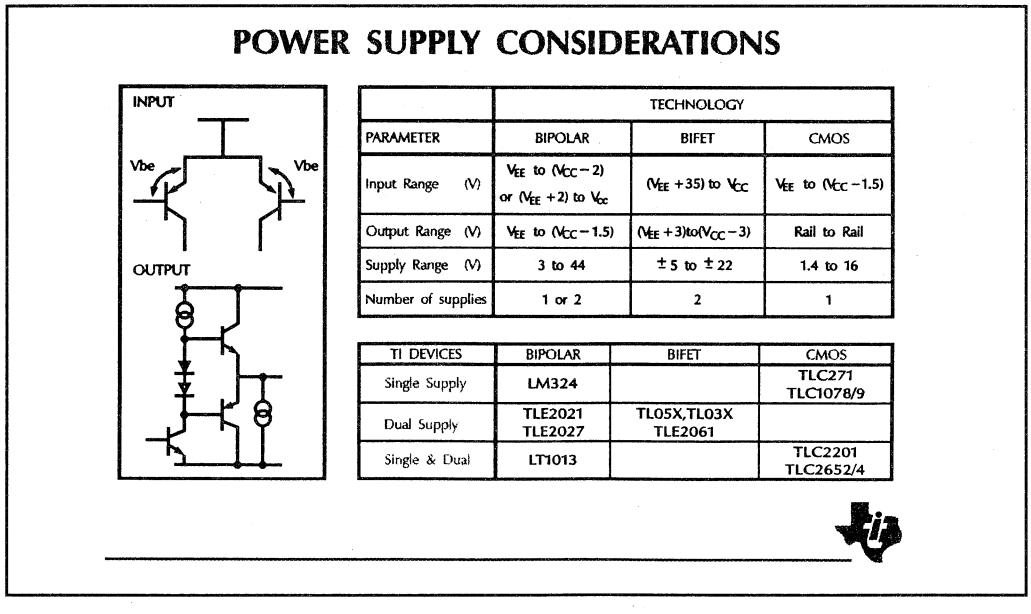
Figure - 39 Accelerometer interface

The charge yielded by the acceleration transducer (B&K Type 4384) is converted into a proportional voltage by the amplifier A1 and A2. Adjusting the sensitivity of charge amplifiers cannot simply be done by trimming the feedback capacitor. An alternative method is shown, where A2, sitting in the negative feedback to A1 can adjust the effective value of C_F by changing the closed loop gain with a standard variable resistor. The effective value of C_F can be varied within the range 1:10 by P1. Due to the capacitive feedback, the length of the transducer cable has a negligible influence on the calibration. The output amplifier, A3 provides a scaling factor within a range of 1:10. The total range covered with the values shown is 1mV/pC to 100mV/pC.

TLE2021 Features

Offset Voltage	... 100µV max
Supply Current	... 200µA
Slewrate	... 0.9V/µs
Bandwidth	... 2.1MHz





	TECHNOLOGY		
PARAMETER	BIPOLAR	BIFET	CMOS
Input Range (V)	V_{EE} to (V_{CC} – 2) or (V_{EE} + 2) to V_{CC}	(V_{EE} + 35) to V_{CC}	V_{EE} to (V_{CC} – 1.5)
Output Range (V)	V_{EE} to (V_{CC} – 1.5)	(V_{EE} + 3)to(V_{CC} – 3)	Rail to Rail
Supply Range (V)	3 to 44	± 5 to ± 22	1.4 to 16
Number of supplies	1 or 2	2	1

TI DEVICES	BIPOLAR	BIFET	CMOS
Single Supply	LM324		TLC271 TLC1078/9
Dual Supply	TLE2021 TLE2027	TL05X,TL03X TLE2061	
Single & Dual	LT1013		TLC2201 TLC2652/4

Figure 41 - When is an op amp single or dual rail?

Operational amplifiers are required to operate with many different supplies. Circuits may be battery powered and required to run off a single 2V supply or they may have +/-22V or more in an instrumentation application. The available power supply affects the choice of op amp.

Single supply op amps will normally need to operate from a 5V supply and will typically require an input common mode range down to the negative rail and an output that swings near to ground. It is unlikely a system running from +/- 15V will need such performance.

An op amp with a common mode input range down to the negative rail can easily be designed using a bipolar process. PNP transistors will ensure the input can swing down to the negative rail, or below, without causing problems. A good output swing is not as easy to achieve. Many bipolar devices are optimised for dual supply operation, ie capable of sinking and sourcing current - this therefore means the output will not normally swing to the negative rail. If a device is optimised for single supply, like the LM324, when they do operate with dual supplies their output suffers from crossover distortion. Bipolar devices that are suitable for both single and dual supplies are uncommon.

Bifets have been designed for dual supply operation. Their common mode input range reaches (and sometimes exceeds) the positive rail, the output will normally swing within 3V of each supply. They operate from a wide range of supplies (+/-3.5V to +/-22V for the newer designs) and are optimised for AC performance.

CMOS devices, like the industry standard LinCMOS, have been specifically designed for single supply operation. Their input range goes below the negative supply and the output can swing within microvolts of ground. The positive output swing typically exceeds 3.5V for the standard TLC27X series and new devices such as new TLC2201 have an output that will swing to +4.7V with a 5V supply. Unlike bipolar designs, CMOS devices with push pull outputs can also perform well with both single and dual supplies. A limitation in some dual supply applications however is their maximum operating voltage, typically 18V.

A common problem with many devices is that they suffer from 'phase inversion'. If the input swings beyond the power rail, the ouput will change state and swing to the opposite rail. Devices such as the LM324 and old Bifets are known for this problem. Newer products like the TLE2021 family have been designed to avoid this.

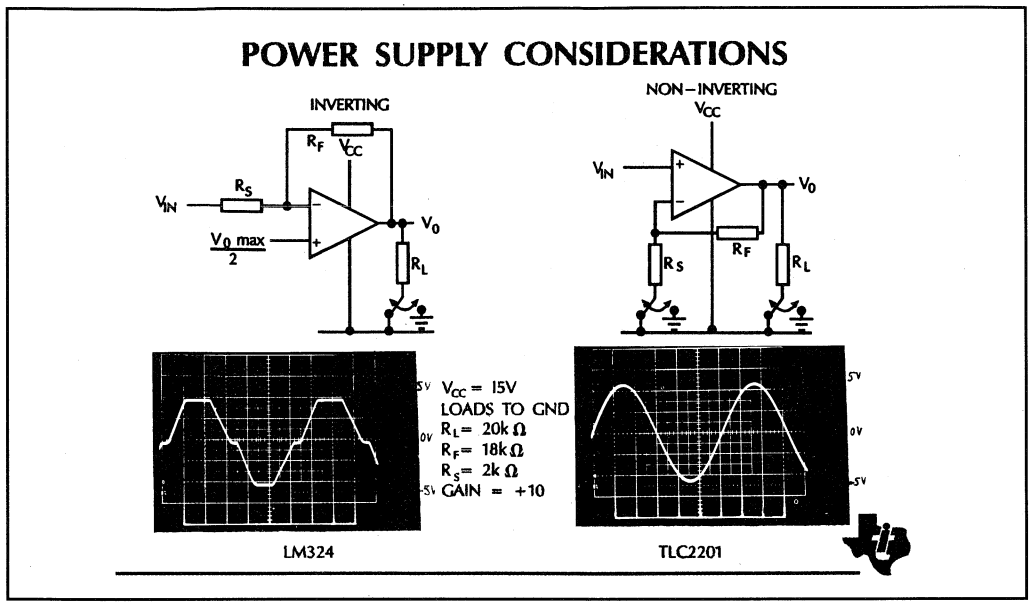


Figure 42 - Single supply application consideration

In single supply circuits consideration must be paid to the feedback resistor and the point of reference at the output. In inverting applications the non-inverting input is placed at a voltage to optimise the output swing. To avoid the output stage having to sink current the load will normally be connected to ground. The feedback resistor is therefore connected to a voltage above ground which in turn means the output stage will have to sink current. If the feedback resistor is small relative to the load, it may demand too much current and cause distortion on the output. A large feedback resistor should reduce this problem. This also applies to some non-inverting configurations when the feeback resistors are not referred to the negative rail.

Distortion is common when single supply devices have to both sink and source current. They have been designed to source current even when close to the negative rail and this compromises the ability to sink current. Differences between the transistors in the output stage can cause positive and negative signals to have different gains. Also, delays in the output stage between one transistor turning on and another turning off can cause crossover distortion. Basically, single supply op amps are not normally designed to both sink and source current.

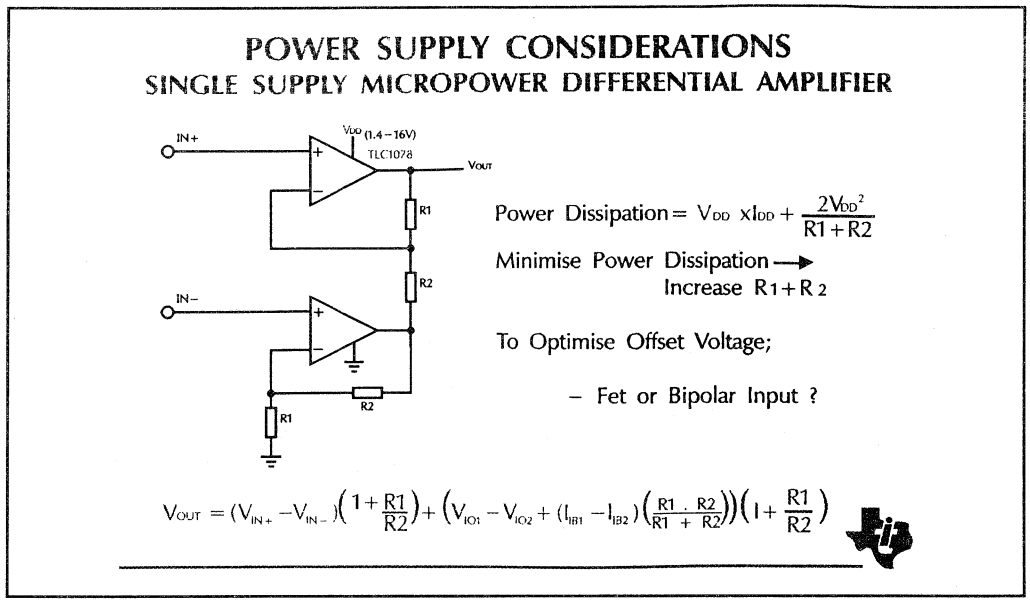


Figure 43 - Micro-power precision application

In low power precision circuits, care must be taken to choose the correct components. If a device requires only microamps it is essential the external resistors do not comsume too much power. If the resistors chosen are too large, the effect due to bias currents on the overall offset can impact the precision of the system.

The circuit above shows a low power system. The key care-abouts are low power consumption and precision. To achieve the required level of precision, the first choice of op amp may have been low power bipolar. If then the resistors are made a few megaohm to optimise power dissipation, the effect off the input bias currents on these resistors causes the circuit accuracy to be degraded.

The offset equals:

$$V_{OS} = V_{IO1} - V_{IO2} + (I_{IB1} - I_{IB2}) \left(\frac{R1 \cdot R2}{R1+R2} \right)$$

Ideally the second term should go to zero. An ideal choice in this application is the TLC1078. Its minimum operating voltage is 1.4V, its supply current at this voltage is less than 10mA and the maximum offset voltage is 450µV. This offset will stay at this value even at low supply voltages.

TLC1078 Features

V_{CC} Range	... 1.4 to 16V
I_{CC}	... 25µA @ 5V
	... <10µA @ 1.4V
Offset Voltage	... 450µV max
Bias Current	... 0.1pA typ @ 25°C

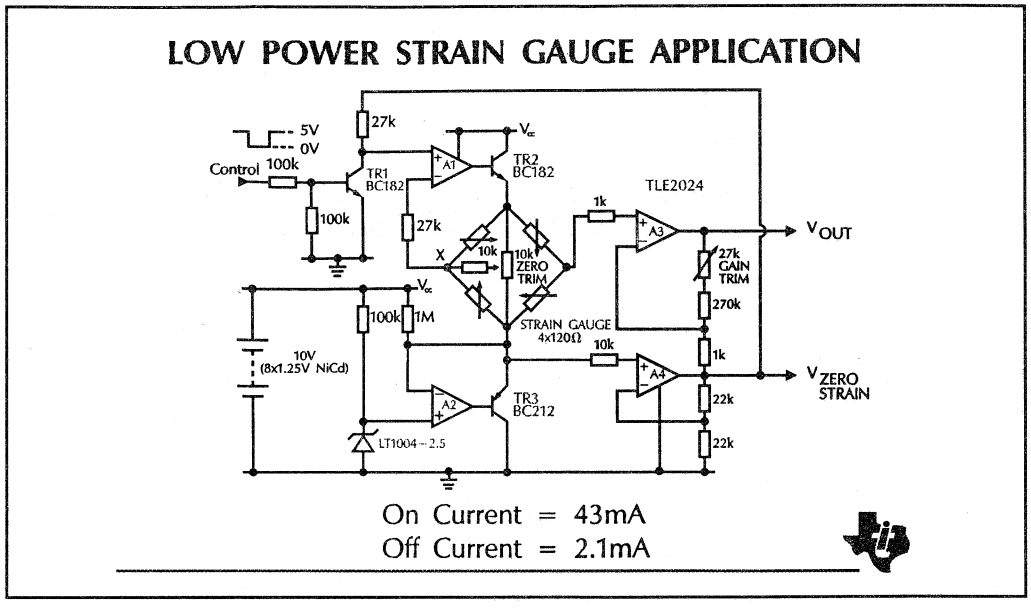


Figure 44 - Low power strain gauge signal conditioner

In many applications the power consumption of the external circuitry dominates the total circuit.

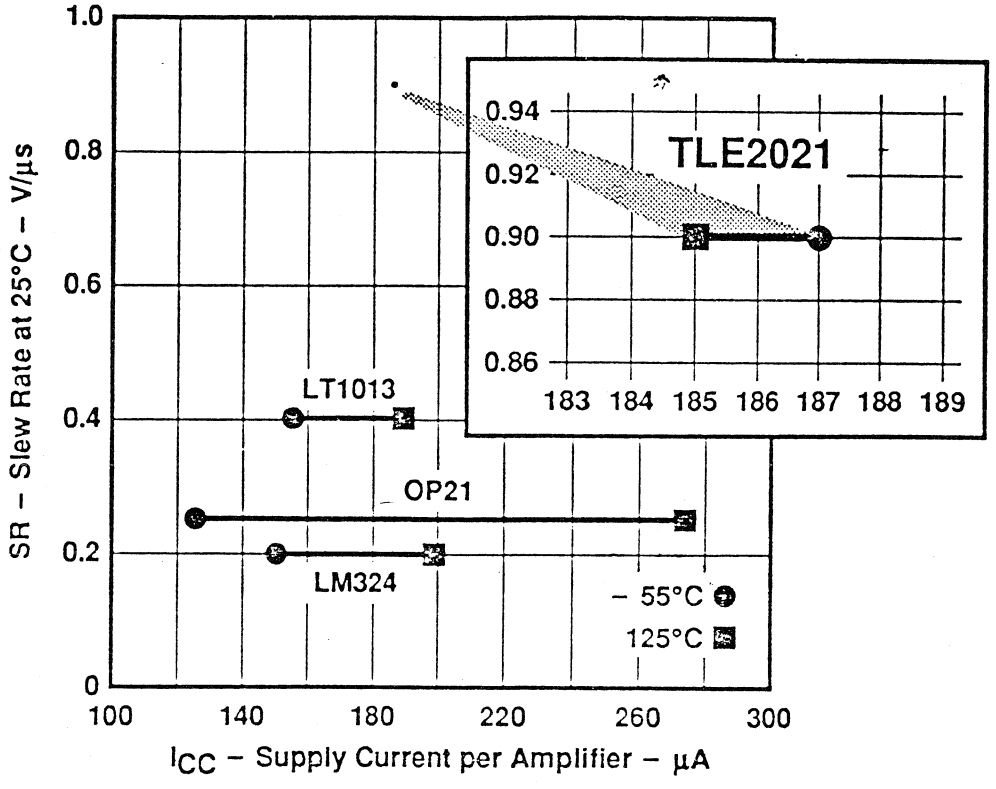
Strain gauges have typical impedances of 120Ω to 350Ω. In order to monitor their maximum 2% change in value, large voltages are normally placed across them. The result is a significant level of supply current.

This application shows how the strain gauge can be turned on and off to reduce the total supply current. The circuit is configured such that an accurate reference is quickly applied to the strain gauge after initialisation. This reference, the LT1004-2-5 from TI consumes only 20µA. The TLE2024 is used to buffer the reference voltage amd amplify the signals from the strain gauge. The effect of mismatches between the strain gauges must be trimmed out. A further advantage of the TLE2024 Excalibur op amp is its long term stability; its V_{10} drift with time is typically 6nV/month!

TLE2021 Features

Offset Voltage	... 100µ V max for B grade
Offset Drift	... 0.006µ V/month typ
	... 2µ V/°C
I_{CC}	... 250µA max
I_{CC} Drift	... <50µ A over - 55 to + 125°C

TLE 2021 STABILITY



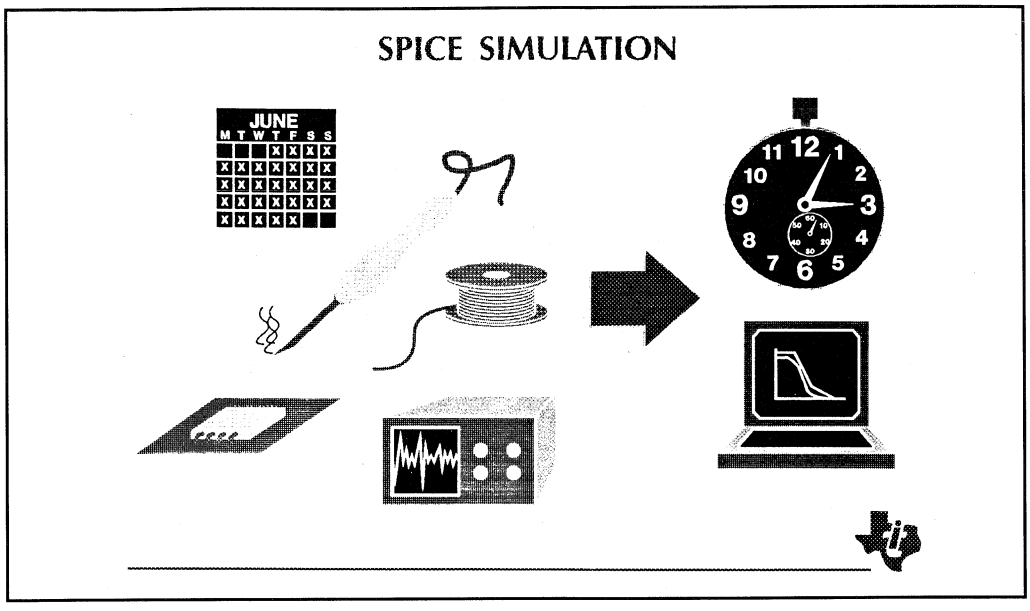


Figure 45 - Computer simulation of electronic circuits

Computer simulation of circuits is becoming increasingly common. With advances in computing technology it is now possible to get useful results from a simulator running on a desk top or even a lap top computer.

Spice was first developed at Berkley, California in the early 1970s and remains by far the most popular analogue simulation programme.

PSpice is a small system version of the proven Berkley Spice II simulator which gives Spice power to those with workstations and PCs. Spice is most useful for experimenting and trying out new circuit designs without resorting to soldering irons, oscilloscopes etc. However simulation should not replace the thorough bench testing of prototype circuits.

TI has recently made available macromodels of all its op amps. Yhese simplified circuits defined in the standard Spice format, model the response of the real op amp. They were designed to model the most important op amp parameters with reasonable accuracy and be simple enough to give run time suitable for interactive use.

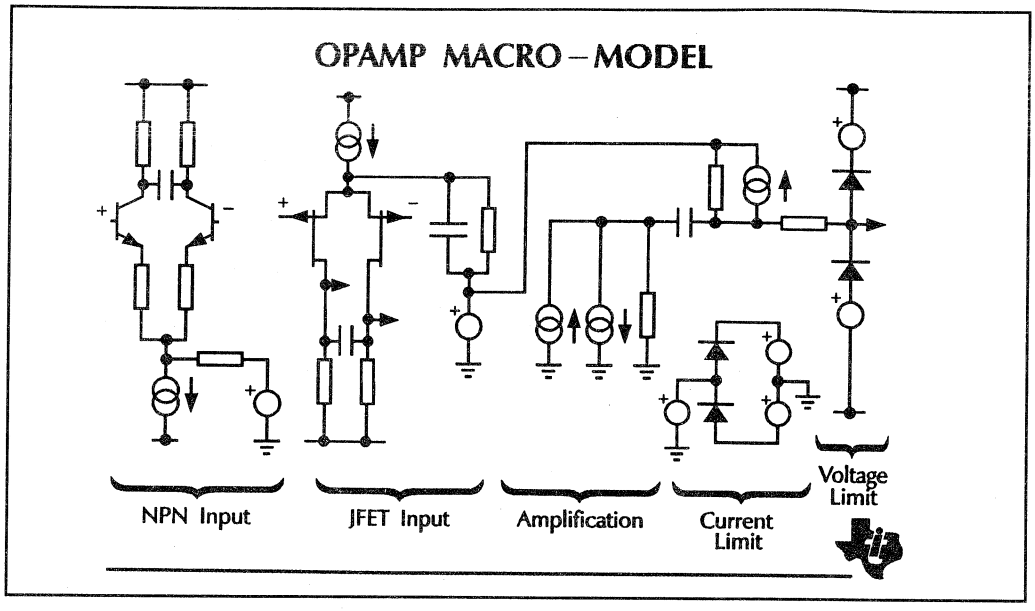


Figure 46 - Op Amp macromodel

The model adopted by TI is based on the industry standard Boyle's model. This model contains transistors, diodes, resisitors and capacitors, along with ideal voltage and current controlled current sources to mimic the operation of a real op-amp.

The input stage of the model is a simplified version of a typical real input stage. The current source has been replaced by an ideal current source, but the input transistors (Bipolar or FET) are retained. This allows modelling of the change in slew rate with differential input voltage. The subsequent stages of the real op amp are replaced with ideal amplifiers to model the gain and frequency response of the op amp. The output stage of the model includes the effects of limited output voltage and currents.

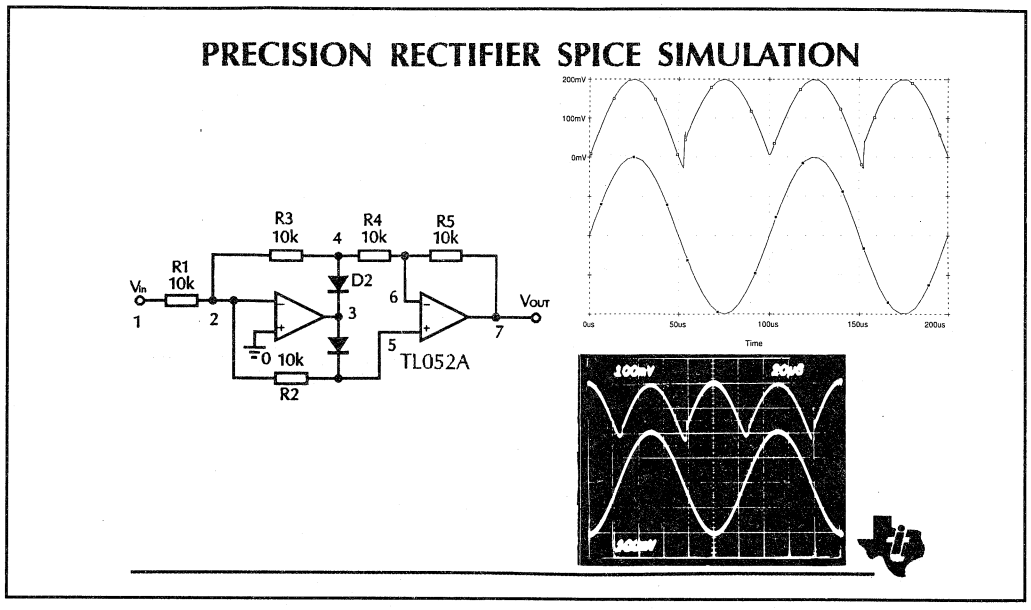


Figure 47 - Example using Spice

As an example of modeling a real circuit, the graphs compare the results from a real lab experiment and the output of the PSpice simulation. The circuit is the precision rectifier presented earlier. The simulation was done using the transient analysis and took only seconds to run on a PC.

Circuit Listing

```
*Op Amp Rectifier

x1 0 2 8 9 3 tl052
x 2 5 6 8 9 7 tl052

r1 1 2 10k
r2 2 5 10k
r3 2 4 10k
r4 4 6 10k
r5 6 7 10k

d1 3 5 dx
d2 4 3 dx

vp 8 0 dc 15
vn 9 0 dc -15

vin 1 0 sin (0 200m V 10kHz)

.model dx d (is=800e-18)
.inc c:\dos\spice\timodels\t1052.mod

.tran 0.1us 200us

.end
```

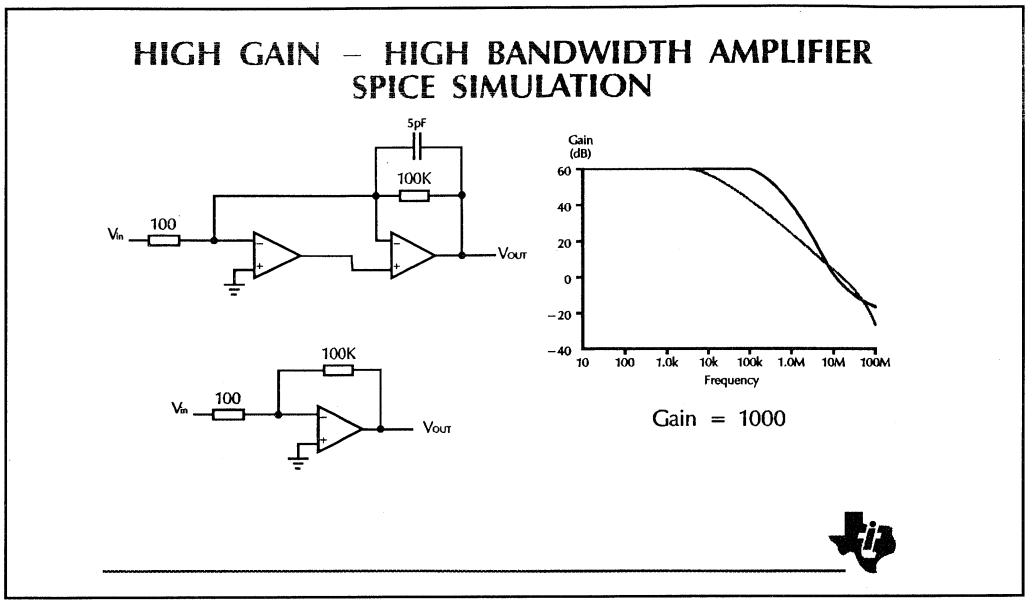


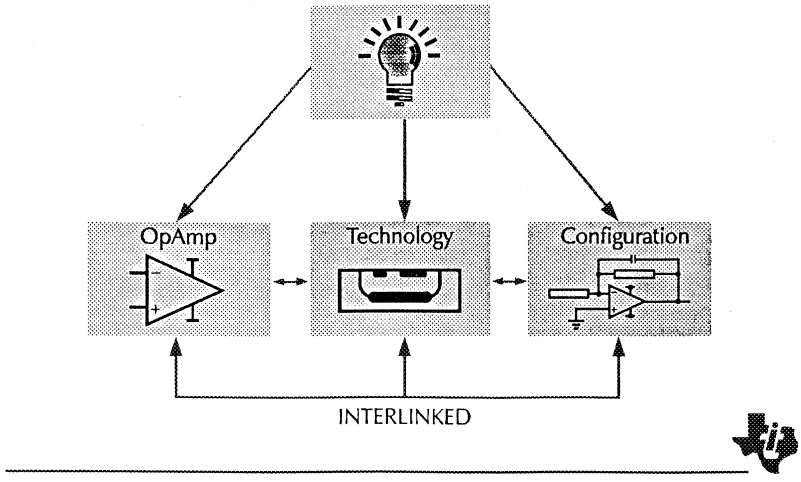
Figure 48 - Modelling a high performance composite amplifier

In this example, Spice was used to simulate the AC frequency response of a composite amplifier. This configuration is useful for high gain amplifiers and precision integrators in filters. Two op-amps are combined to give a wide bandwidth, very high gain amplifier. This bandwidth is wider than that which can be obtained from a single op-amp. Similiar results could be achieved by cascading two lower gain amplifiers. However, this would require twice as many precision resistors and could not be used for an integrator.

Circuit File Listing

```
High Gain Amplifier

* Power Supplies
vp 10 0 dc 15
vn 11 0 dc -15

* High Gain Composite Amplifier
x 1 0 2 10 11 3 tle2027
x2 3 2 10 11 4 tle2027
r1 3 2 100
r2 2 4 100k
c1 2 4 5p

* Standard Inverting Amplifier
r11 1 5 100
r22 5 6 100k
x3 0 5 10 11 6 tle2027

vin 0 1 ac 1m
.ac dec 10 10 100Meg
.inc c;\dos\spice\timodels\tle 2027.mod
.end
```

OPERATIONAL AMPLIFIER – CIRCUIT DESIGN



SECTION 2.
POWER SUPPLY

POWER SUPPLY INDEX

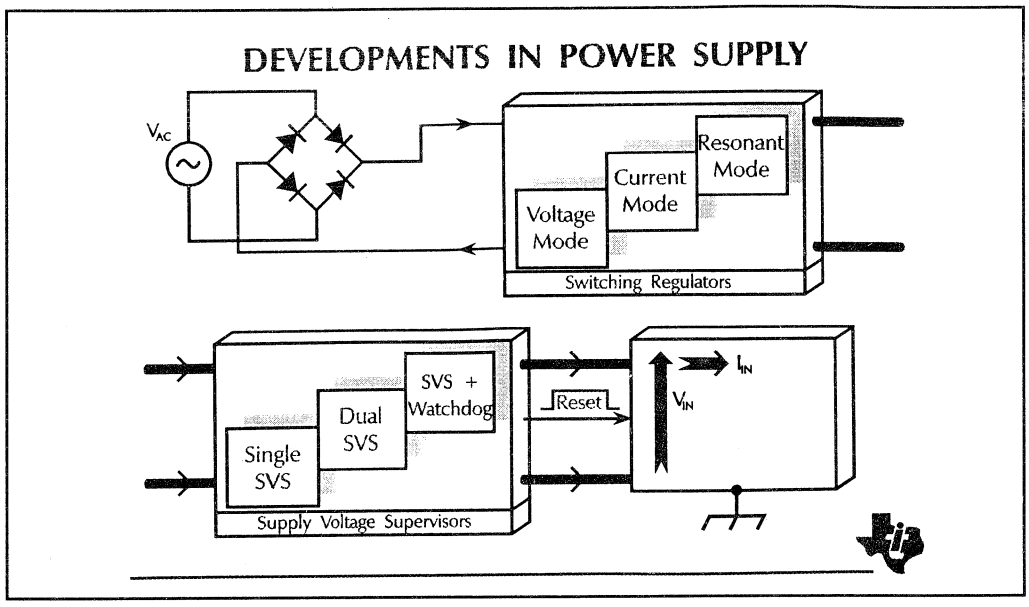


Figure 1 - Developments in Power Supply functions

This section of the seminar will address power supply components, concentrating on two areas of this field - Switching regulators and Supply voltage supervisors.

1.1 **Switching regulators**

Providing a stable ,regulated supply to any electrical system is clearly a fundamental requirement for reliable operation. The development of the first monolithic regulators was a big help to power supply design, making it simpler and more cost effective.

In this section, we show the developments in the area of switching regulators, explaining how they differ from Linear series regulators, the principles of operation, and the development from voltage mode to current mode. Finally, the theory of the latest form of switching regulator - the resonant converter, is presented.

1.2 **Supply voltage supervision**

In this section , we explore the purpose of supply voltage supervision, and where and how it is used to ensure a system is operating within its correct supply voltage "window".

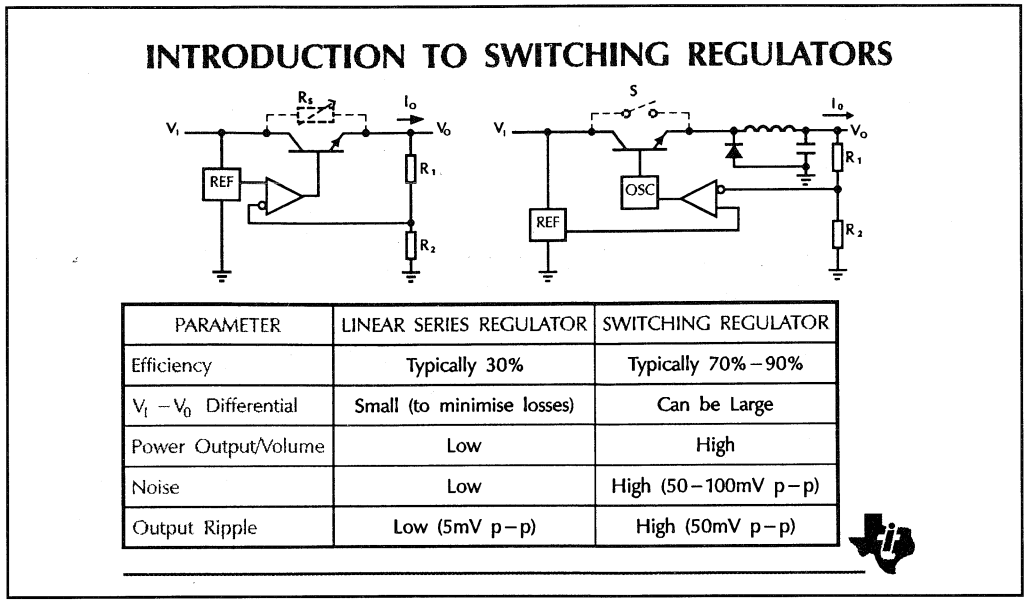


Figure 2 - Introduction to Switching regulators

The function of a voltage regulator is to convert a DC input voltage into a defined, stable output voltage and to maintain the output over a wide range of load current and input voltage conditions. To acheive this, a typical regulator consists of the following elements;

1. A voltage reference (Vref) to provide a fixed voltage level.
2. A sampling element to monitor the output voltage
3. An error amplifier for measuring the difference between the actual and desired output voltage.
4. A power control element to deliver the required energy from input to output.

The first three functions are broadly the same for any type of regulator. However, the control element is what distinguishes the different types. For a Linear or Series regulator, this control element is normally a transistor. Control is provided by varying the value of the series resistance of this transistor to allow more or less current through from input to output.

With a switching regulator, the control element is also a transistor , but it is used in a different way. In this case, control is provided by "chopping" the input voltage to pass energy from input to output in proportion to the duty cycle . The primary advantage of this technique is that the active element (the transistor) is either fully saturated or fully off - in both cases power dissipated in the switch is minimised. Therefore, the switching regulator operates at higher efficiency than its series counterpart. Typically, a switching regulator operates at 70%-90% efficiency, compared to the 30% of a series regulator.

Another advantage of the switching regulator is a decrease in size, weight and hence cost per Watt of output power. This is because by operating at higher switching speeds, the size of the passive components required is reduced by a factor of about 8 times for switchers operating over 100kHz.

The disadvantage is that the regulators are more complex and require more complicated supporting circuitry. The switching process also introduces high frequency electrical noise although this will be attenuated to some extent by the connecting cables and filter capacitors on the output. As switching frequencies increase, this noise also becomes easier to filter out. Finally, the switchers tend to introduce more ripple on the output voltage.

The relative pros and cons of switching regulators as compared to series regulators are summarised in the table below. As a general rule, the switching regulators are of most benefit in applications that require higher power requirements, where the input to output differential is large and where efficiency of the power supply is of utmost importance.

Table 1. Pros and Cons of switching regulators compared to Linear regulators

Advantages	**Disadvantages**
High Efficiency	Electrical noise
High power/weight ratio	More complex design
High input to output differential	Higher output ripple

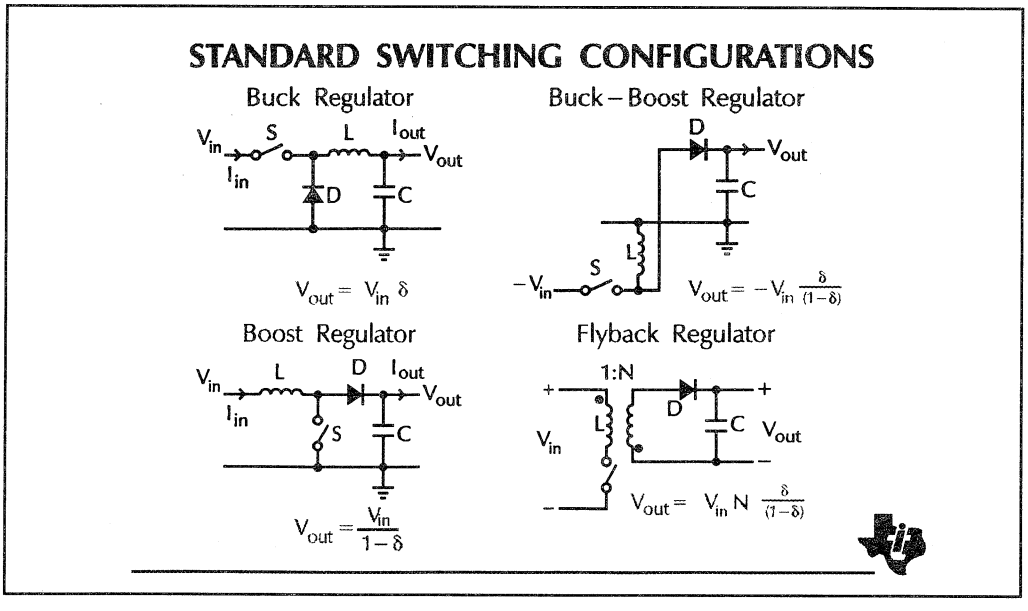


Figure 3 - Standard switching configurations

We will now examine the basic switching configurations where switching regulators can be used. In each case, the output voltage depends upon the duty cycle of the circuit to a first approximation. The duty cycle is defined as the ratio of the time for which the switch is closed (t_{ON}) compared to the total period of the oscillator driving the switch (t_{ON}+ t_{OFF}). The theoretical limits on this can vary from 100% (when the switch is permanently closed) to 0%, (when it is permanently open), although in practice, it may not be possible to use the complete range. The Duty Cycle δ is therefore defined as

$$\delta = (t_{ON}) / (t_{ON}+t_{OFF})$$

In all the following topologies, the principle used is that the output voltage is maintained at a constant value by keeping a constant charge on the capacitor. Energy is delivered to the load in each cycle by the output current I_{OUT}. This is replaced by energy delivered from the input via the inductor which acts as a storage element.

In each case, the first order approximations for the output voltage are derived making the assumption that the passive elements are ideal - i.e. they contain no series resistance which dissipates power. The forward voltage drop of the diode is also assumed to be zero to a first approximation.

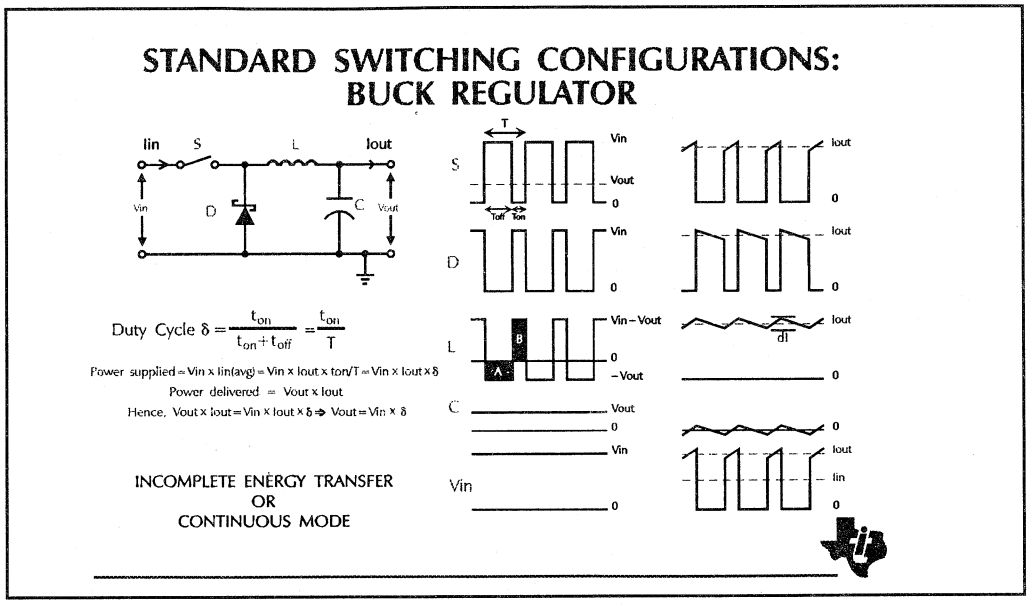


Figure 3.1 Buck Regulator

This first diagram shows the Buck or Series regulator and its associated voltage and current waveforms.

a) Switch closed for time t_{ON}

The change in the current flowing in the inductor is given by:

$$V=L\ dI/dt \qquad (V_{IN}-V_{OUT})\ t_{ON}/\ L = dI \qquad 3.1.1$$

For steady state , the increase dI during t_{ON} should be matched by an equal decrease during t_{OFF}. Therefore we can write

$$\Sigma\ dI = 0 \quad \text{so } \Sigma\ V\ .\ t\ /\ L = 0 \ \text{ and } \ \Sigma\ V\ .\ t\ = 0 \qquad 3.1.2$$

Hence, the product of the voltage across the inductor and t_{ON} should be the same as the product of the voltage across the inductor and t_{OFF}. This is indicated on the diagram of the inductor voltage where area A is the same as area B.

b) Switch open for time t_{OFF}

When the switch is open, the collapsing magnetic field in the inductor creates a back emf which forward biases the diode and allows the stored energy to flow out into the capacitor.

$V=LdI/dt \qquad -V_{OUT}t_{OFF} / L = -dI$ 3.1.3

Therefore, from 3.1.1 and 3.1.3 , $V_{OUT}\, t_{OFF} = (V_{IN} - V_{OUT})\, t_{ON}$ 3.1.4

Simplifying, $V_{OUT}= V_{IN}.t_{ON} /(t_{ON}+ t_{OFF}) = V_{IN} .\delta$ 3.1.5

Since δ cannot exceed 1, the Buck regulator always ***steps down*** the output voltage. However, since the circuit contains only components that are theoretically "lossless", there is no power dissipation in the circuit and the input power equals the output power. Therefore

$$V_{IN}. I_{IN}= V_{OUT}. I_{OUT} \text{ or } I_{OUT} = I_{IN} . (V_{IN} /V_{OUT}) \qquad 3.1.6$$

and the output current is increased by the ratio of the voltages. Note that this expression refers to the average value of I_{IN}. As can be seen from the current waveform, the peak value of I_{IN} is equal to I_{OUT} + 1/2 dI.

The diagrams show the circuit operating in Incomplete Energy Transfer (IET) or Continuous mode. These names derive from the operation of the inductor. Since the current in the inductor never falls to zero, i.e. it is continuous, there is always some energy stored in the inductor . This requires the use of a larger inductor than would be the case if there were Complete Energy Transfer (CET) on each cycle, so that the inductor current reached zero before the start of the next cycle. However, the CET mode of operation needs the circuit to handle far higher peak currents for the same average I_{OUT}, and there is also much larger current ripple on both the inductor and the capacitor.

3.2 Boost Regulator

In this configuration, energy is delivered from the input and is stored in the inductor whilst the switch is closed. The diode is reverse biased since the input voltage is lower than the output and so no current flows into the load at this time.When the switch opens, the inductor tries to preserve the collapsing magnetic field by creating a back emf which forward biases the diode and forces it into conduction. In this way, a current pulse is delivered into the capacitor and the load. This current pulse has a higher peak than the average output current. In this way , energy from the line plus stored energy in the inductor is delivered with each pulse.

a) Switch closed for time t_{ON}

$V_{IN}. t_{ON} / L = dI$ 3.2.1

b) Switch open for time t_{OFF}

$(V_{IN} - V_{OUT}) . t_{OFF} / L = -dI$ 3.2.2

Therefore $V_{OUT} = V_{IN} (t_{ON} + t_{OFF})/ t_{OFF} = V_{IN} / (1 - \delta)$ 3.2.3

$$V_{OUT} = V_{IN} / (1 - \delta)$$

and since $\delta < 1$ this means that it ***steps up*** or ***boosts*** the output voltage.

3.3 Buck-Boost regulator

The Buck-Boost regulator operates in a similar manner to the Boost converter, but in this case only the energy delivered to the inductor is passed on when the switch is opened. The Buck-Boost configuration is used to invert the input voltage and can either step up or step down the magnitude of the voltage depending on the duty cycle .

a) Switch closed for time t_{ON}

$$-V_{IN} \cdot t_{ON} / L = dI \qquad 3.3.1$$

b) Switch open for time t_{OFF}

$$-(V_{OUT}) \cdot t_{OFF} / L = -dI \qquad 3.3.2$$

Therefore $V_{OUT} = -V_{IN} \cdot t_{ON} / t_{OFF} = -V_{IN} \cdot \delta / (1 - \delta)$ 3.3.3

$$V_{OUT} = -V_{IN} \cdot \delta /(1 - \delta)$$

3.4 Flyback regulator

The flyback regulator is a development of the Buck-Boost converter that uses a transformer to deliver the energy from input to output. While the switch is closed, current builds up in the primary windings so storing energy. The polarity of the windings ensures that the diode is reverse biased. When the switch is opened, the stored energy is delivered to the load.

a) Switch closed for time t_{ON}

$$V_{IN} \cdot T_{ON} /L = dI \qquad 3.4.1$$

b) Switch open for time t_{OFF}

$$-(V_{OUT}) \cdot t_{OFF} / (N.L) = dI \qquad 3.4.2$$

Therefore $V_{OUT} \cdot t_{ON} / t_{OFF} = V_{IN} \cdot N \cdot \delta / (1- \delta)$ 3.4.3

$$V_{OUT} = V_{IN} \cdot N \cdot \delta / (1- \delta)$$

There are therefore two controllable parameters to adjust the output voltage - the duty cycle and the turns radio. Due to this, the flyback converter can provide either current gain or voltage gain. There is a disadvantage in that the output ripple current is higher than the other configurations but this design also offers isolation of the output from the input.

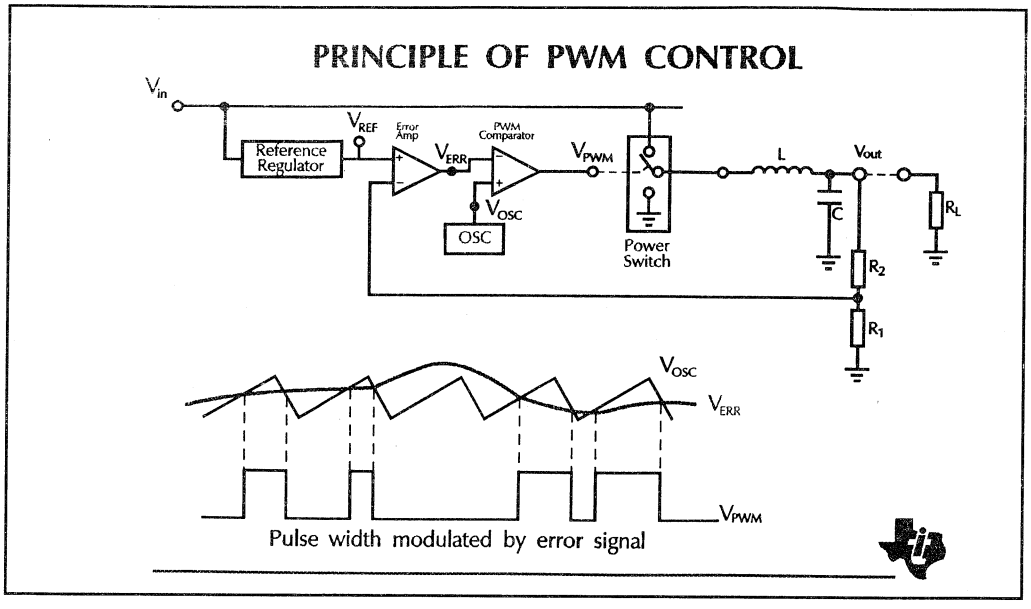


Figure 4 - Pulse width modulation control

The diagram shows the principle of pulse width modulation. As we have already seen , the output voltage can be controlled by controlling the duty cycle of the switching element. Pulse width modulation or PWM provides the means to do this.

As was shown in the introductory foil, control is provided by a feedback loop from a sampling element on the output, (usually a potential divider as shown) which is compared to the known reference voltage. The difference between the actual and desired output is then generated by a differential amplifier which produces an error signal in proportion to this difference. This error signal is in turn then compared to a voltage ramp produced by an oscillator at the input to a comparator. The frequency of this oscillator is normally controlled by an external timing capacitor chosen by the user.Whenever the magnitude of the voltage ramp exceeds that of the error signal, the comparator output is high, activating the power switch . Similarly, when the ramp is below the error signal, the output is low and the switch is turned off. In this way, a series of pulses of magnitude V_{IN} is passed to the LC lowpass filter and hence to the output. The width of these pulses (and hence the duty cycle) is modulated by the error signal.

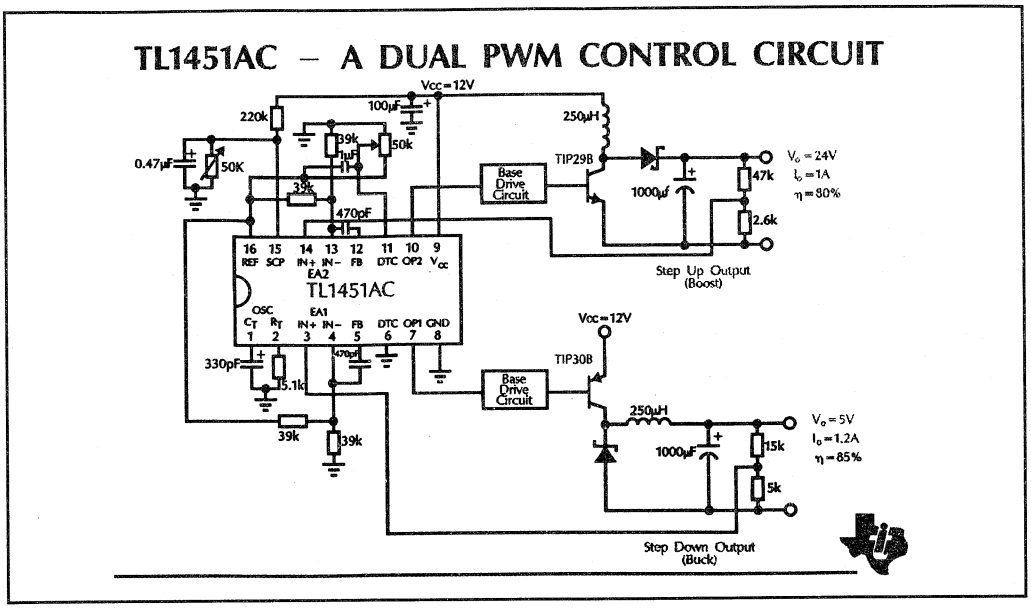
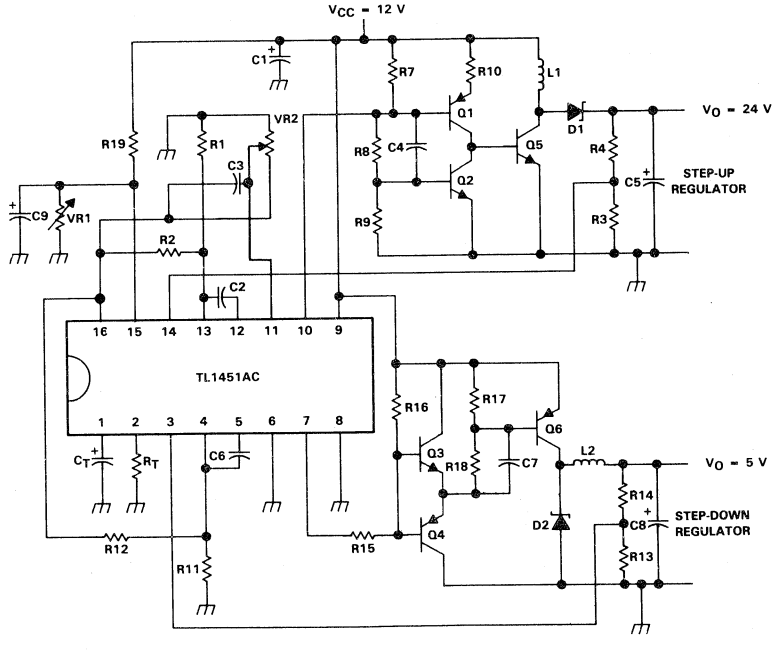


Figure 5 - The TL1451 -A dual PWM control circuit

This diagram shows an example of a device that incorporates all the features necessary to implement two separate PWM control systems in a single package. The TL1451AC is designed for power supply control and is shown here providing two regulated supply voltages from a single 12v d.c. input. The diagram is a simplified version of the full schematic shown below.



In this case, the chosen outputs are 24v at 1A and 5v at 1.2A , produced using a boost and a buck topology respectively. These values are defined by the potential divider chains on the output , with the resistor values chosen in each case to provide a feedback of 1.25v to the non-inverting input of the error amplifiers at pins 3 and 14 when the output voltage is at its correct value. This feedback is compared with the value at the inverting input (pins 4 and 13) which is chosen to be half the value at the reference output pin 16.

The TL1451AC has a 2.5v internal reference which provides a stable supply for the device's internal functions and can also source up to 10 mA for additional external load circuits. The output is provided by two open collector Darlington stages which can sink up to 20 mA and show a saturation of less than 2v at 10 mA. For this application, additional base drive to the power transistors in the output stage is necessary . The frequency of operation is controlled by the capacitor and resistor on pins 1 and 2. The capacitor is charged and discharged by a constant current whose value is determined by the resistor.This produces a triangular waveform that is designed to vary between 1.4V and 2V. In this application, the values of R and C are chosen to produce a 330kHz operating frequency.

TL1451AC Dual PWM control circuit

- **O Complete PWM control circuitry for two independent switching regulators**
- **O Internal undervoltage lockout protection**
- **O Wide supply voltage range 3.6V to 40V**
- **O Low quiescent supply current 2.4mA max**
- **O Wide frequency range . . . . to 500kHz**
- **O Variable dead time control from 0% to 100%**
- **O Stable 2.5V reference**

The TL1451AC also incorporates some other features designed to offer greater control. The first of these is dead time control. The "dead time" is the period of time in each cycle when the PWM control is overridden and the output transistors are switched off. This is acheived using another input to the PWM comparator at pins 6 and 11. If the voltage at these pins exceeds that of the oscillator output, the output transistors are switched off irrespective of the error voltage signal. By setting a level between 1.4V and 2V, the dead time can be controlled from 0% to 100% of the cycle.

This is useful in a push-pull configuration when the outputs operate out of phase with each other on two halves of a centre tapped transformer. In this case, it is essential that there is no time when both outputs are switched on together since this would create a short circuit from the supply rail to ground. Dead time is employed here to ensure there can be no overlap. In the example shown, a potentiometer (VR2) is used to provide about 10% dead time, which is desirable for this output.

Dead time control also provides the means to include a soft start up capability. Soft start cushions the output at start up when the large capacitor on the output needs to be charged up . Without it , the error feedback would be very large, forcing the output to be on for 100% of the cycle. With C3 tied to the reference pin as shown, the voltage on the deadtime control pin starts at 2.5V and then decays as C3 charges up . In this way the deadtime falls from 100% at start up to 10% when the circuit has stabilised.

An undervoltage lockout (UVLO) circuit monitors the supply voltage and overrides operation if it falls below the minimum of 3.6V. This ensures the reference regulator and other circuitry stays within its operating specification and prevents faulty operation of the device.

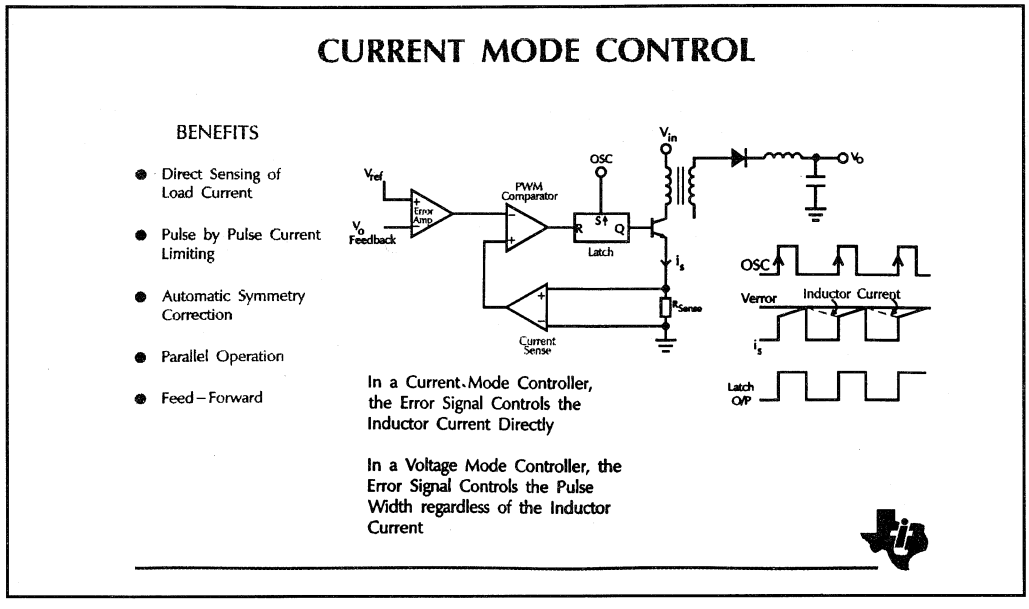


Figure 6 - Current mode control

Current mode control is based around a dual control loop system. The inner loop is the current control. The current flowing from the input, through the inductor and the output transistor when it is switched on, is converted to a voltage by a low value resistor R_{SENSE}. This provides direct feedback of the current flowing in the inductor . This signal is fed back to the PWM comparator , where it is measured against the error signal generated by the outer loop. This loop compares a fraction of the output voltage with the internal reference and provides an error signal in proportion to the difference between the desired and actual output voltage. This error signal is the same as is used in a Voltage mode converter.

In this way, the drive to the output transistor from the latched Flip-Flop is turned off when the sensed inductor current reaches the limit set by the V_{ERROR} signal. Hence, the error signal controls the Inductor current directly to provide inherent pulse by pulse current limiting.

Benefits of current mode control

Direct sensing of load current - Because the load current is measured directly and not just the load voltage, the current mode controller can respond very quickly to variations in the load. Similarly, if the line (input) voltage changes, this has a direct effect on the measured current. Since the current is measured directly, the output is kept on until the current reaches the V_{ERROR} limit so that the correct amount of energy is delivered to the load to maintain the output voltage.

Current compared to error signal - As above, the current is measured directly. Therefore, the output will be shut off in a short circuit condition or if the inductor saturates. With

voltage mode control, the peak current can rise to a damaging level in a short circuit condition as the device tries to maintain the output voltage.

Automatic symmetry correction - When a device is used in a push-pull configuration, two halves of a centre tapped transformer are used. The magnetic characteristics of these may be different so that even though the voltage across each half is the same, the current drawn may be very different leading to saturation of one half of the core whilst the other half is being "under-driven". In a current mode set up this is prevented because the current flowing in each half is monitored directly.

Parallel Operation - In a similar manner to the above, since both current and voltage are monitored, power is shared equally between a number of modules operating in parallel. This makes efficient use of a series of devices operating together in parallel to provide additional current capacity.

Feed Forward - Variations in the line voltage are automatically corrected for by the current sense amplifier as explained above. Therefore the dynamic range of the error amplifier is used to maximum effect to measure variations in the load.

Current mode control is best operated in Complete Energy Transfer (Discontinuous) mode. Any change on the input voltage changes the peak input current and hence the energy stored by the inductor. In CET mode , all this energy is transferred to the output . In IET mode however, the current in the inductor doesnt fall back to zero, so that there is a difference between the energy transferred into the inductor and the energy transferred out. This becomes a ripple on the output as a feedthrough from the input ripple.

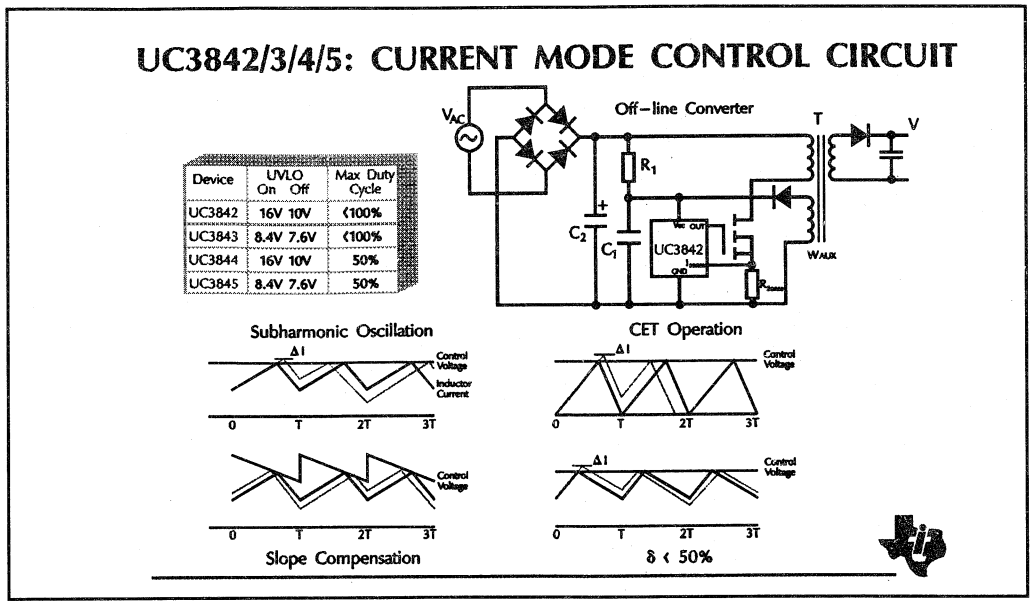


Figure 7 - The UC3842/3/4/5 family of current mode PWM controllers

The UC3842 family of devices offers a compact solution to current mode control with all its associated benefits. The family contains four devices which are distinguished by two main features:

7.1 UVLO (Under voltage lock out)

Under voltage lock out sets defined limits for operation so that the device shuts down if the input is not sufficient to support correct output. The UC3842 and UC3844 have a switch on voltage of 16V and then will remain on whilst the input is above 10V. This large hysteresis is desirable for an offline converter application using a mains input. It prevents Vcc oscillations when it is powered up, and limits the size of the filter capacitor needed on the input.

However, for lower voltage applications and those using a battery input e.g. automotive, this is not necessary and a smaller hysteresis is more desirable. For these applications, the UC3843 and UC3845 are more suitable.

7.2 Duty Cycle

The duty cycle is defined as the fraction of time the output is on compared to the period of the oscillator. At start up it is generally desirable to be able to approach 100% so as to ramp up the output voltage as quickly as possible. However, in some cases, operating at above 50% leads to instability caused by subharmonic oscillations. By limiting the max duty cycle to 50%, this is avoided. Hence there is an option for the 100% duty cycle parts UC3842/3 or the 50% duty cycle parts UC3844/5. Subharmonic oscillations can also be avoided by imposing a slope on the control voltage as shown. The circuit to generate this slope compensation is included in the device datasheet.

UC3842/3/4/5 current mode PWM control circuit

O PWM control circuit with benefits of current mode control
O Undervoltage lockout with hysteresis
O Low start up current <1mA
O Operates up to 500kHz
O Optimised for offline converters
O Trimmed bandgap reference

The diagram shows the UC3842 in an offline application. Power is delivered to the output using the Flyback configuration. During normal operation, Vcc is maintained by the lower auxiliary winding which is rectified and smoothed by D_1 and C_2. At start up, C_1 must be charged to 16V through R_1 . It is essential to have a low start up current so that R_1 can be made as large as possible to limit power dissipation across it during normal operation.

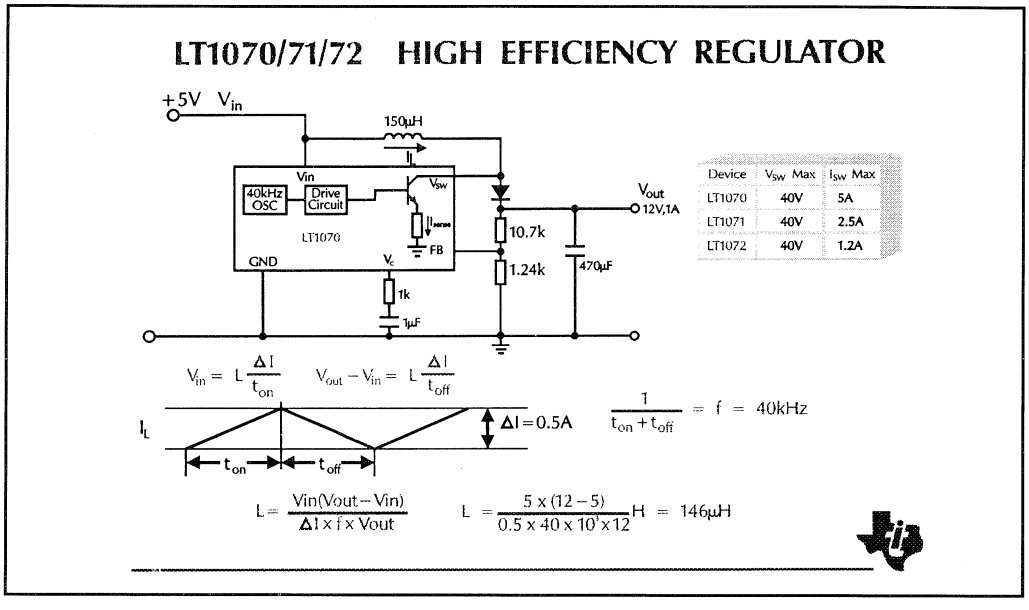


Figure 8 - The LT1070/71/72 High efficiency Switching regulator

The advantages of using switching regulators with their high efficiency and small size have made them increasingly popular. However, they still remain difficult to use and require a number of discrete components as well to build a complete design. The LT1070/1/2 integrates all the functions needed for PWM current mode control into a single package and includes with it a high-current, high-efficiency switch. This gives it the ease of use of a linear Vreg with the inherent advantages of efficiency and regulation provided by PWM control.

The device operates on a wide range of input voltages from 3V to 40V for the standard version and from 3V to 60V for the high voltage -HV version. It requires only 6mA quiescent operating current yet is capable of delivering up to 100W to a load without the need for external power devices. An externally generated shutdown signal on the V_C pin,can put the device into a sleepmode where it draws only 50µA.

There is an on-chip 1.25V reference accurate to 2.5% tolerance. The desired output voltage is set in the usual way by feeding back a fraction via a voltage divider to an error amplifier. An internal 40kHz oscillator provides the clock to drive all the internal timing.

LT1070/1/2 high efficiency switching regulator

- **O Wide supply voltage range 3V to 40V**
- **O Low quiescent supply current 6mA max**
- **O Internal high current switch (5A LT1070, 2.5A LT1071, 1.2A LT1072)**
- **O Shutdown mode 50μA supply current**
- **O Flyback mode for totally isolated output**
- **O Operates in nearly all standard topologies**

8.1 Boost converter

This application shows the LT1070 in a boost converter. Its high level of integration makes the complete circuit much easier to design .The device can operate in this configuration with an input as low as 3V , and an output of up to 50V. R1 and R2 are chosen to set the feedback voltage to 1.25V, with a current down the chain of 1mA. The choice of inductor is a trade off. High values give maximum output power and low ripple but are physically bulky and have slower transient response. The lower values have reduced power and higher ripple but respond to transients more quickly. They can also lead to instability problems if Duty cycle is greater than 50%.

One way to choose the value required is to specify the maximum ripple current in the inductor ΔI.

Remember, for the boost converter

$$V_{IN} \cdot t_{ON} / L = \Delta I \qquad \Rightarrow t_{ON} = L\,\Delta I / V_{IN} \qquad 8.1.1$$

$$(V_{IN} - V_{OUT}) \cdot t_{OFF} / L = -\Delta I \qquad \Rightarrow t_{OFF} = L\,\Delta I / (V_{OUT} - V_{IN}) \qquad 8.1.2$$

Hence $$t_{ON} + t_{OFF} = L\,\Delta I\, V_{OUT} / (V_{OUT} - V_{IN})\, V_{IN} = 1 / f \qquad 8.1.3$$

So $$L = V_{IN} (V_{OUT} - V_{IN}) / (\Delta I \cdot f \cdot V_{OUT}) \qquad 8.1.4$$

Choosing a maximum ripple of 0.5A , and using the other values as shown on the diagram ,

$$L = 5 (12 - 5) / (0.5 \cdot 40 \times 10^{3} \cdot 12) = 146\ \mu H$$

The RC network connected to the V_C pin provides loop frequency compensation. Typically, this circuit operates at up to 90% efficiency.

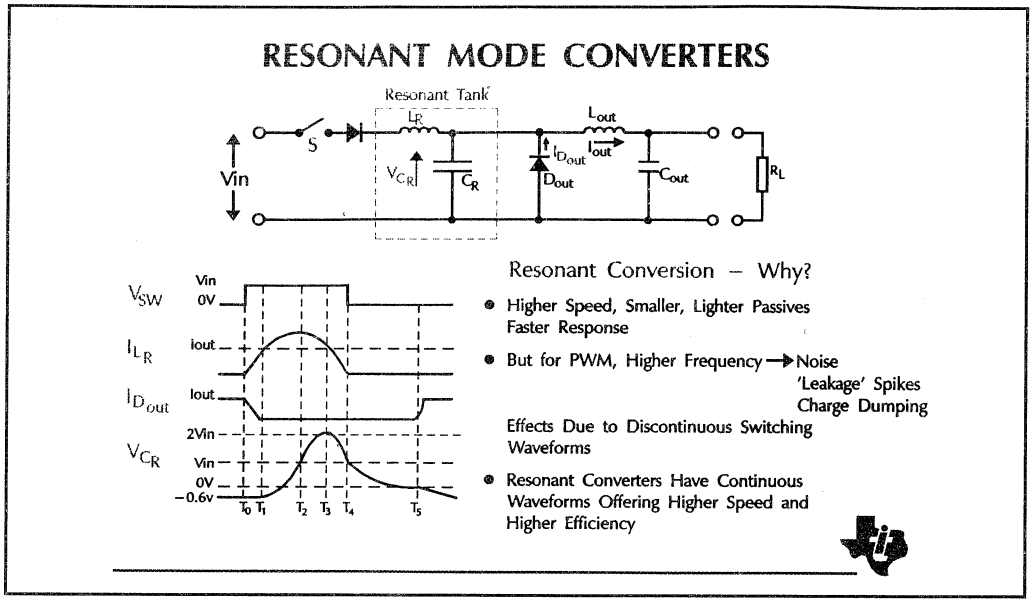


Figure 9 - Resonant mode converters

9.1 High frequency effects in PWM converters - Noise, Spikes and charge dumping

As has already been shown, the advantages of switching regulators are primarily derived from the fact that they can operate at high frequencies allowing the use of smaller, lighter and cheaper passive components. They also provide a faster response to load transients and consequently better regulation of the output voltage.

However, increasing the frequency of operation also brings undesirable effects . The first of these is an increase in electrical noise . Since the switching waveforms of the PWM devices are basically "square" (they are discontinuous) , they contain spectral components with frequencies much higher than the fundamental that create RF noise.

A second problem is that of "leakage " spikes. There will always be parasitic inductance in the circuit in series with the switching transistor and when the switch turns off, this creates ringing in this parasitic inductance . Large voltage spikes are hence created across the switch which may damage it but will certainly create more noise and dissipate energy which is then lost to the load. Snubber circuits can prevent the dangerous overvoltages but they generally do so by dissipating the energy themselves.

Finally , there is a further loss mechanism in the switching transistor itself. When the switch is off, charge is stored in the effective parallel capacitance of the transistor (either the Collector-Emitter capacitance for a Bipolar device or the Drain -Source capacitance in a MOSFET) . At switch on this charge is "dumped" and the stored energy is lost. This effect occurs on each cycle and so is in direct proportion to the switching frequency.

The root cause of all these problems is the discontinuous waveforms used by the PWM converters. The solution lies in using an LC resonant circuit to store the energy pulses and deliver them to the load using either a continous current or a continuous voltage waveform, so avoiding the problems indicated above.

9.2 Principle of resonant converters

The principle of resonant conversion is shown in the diagram. It is assumed that the output filter formed by L_{OUT} and C_{OUT} is sufficiently large that the output current and output voltage remain constant.

In the initial condition, the switch is open and no current flows in the resonant tank formed by L_R and C_R. D_{OUT} is forward biased and supplies the current I_{OUT} into L_{OUT} so that the voltage V_{CR} is equal to -0.6V. When the switch is closed at time T_0 , there is a constant voltage across L_R so that the current in it I_R rises linearly until $I_R = I_{OUT}$ at time T_1.

At this time D_{OUT} becomes reverse biased and switches off. I_R continues to supply I_{OUT} and now also begins to charge C_R. When C_R has become charged to V_{IN}, there is no potential across the inductor and the current peaks at T_2. The inductor current I_R then begins to fall but still charges the capacitor until it falls to I_{OUT} again at T_3 when the charge stored in the capacitor is at a peak. I_R continues to decay back to zero and the capacitor now supplies current to the load as it begins to discharge. At time T_4 the inductor current falls to zero and the switch opens again. Since it both opens and closes with the current at zero , there are no "overlap" losses in the switch.

The cycle is completed as the capacitor is fully discharged until D_{OUT} is forward biased once more at T_5.

With each cycle the energy delivered to the load is the same as that delivered to the capacitor C_R since it is fully charged and discharged in each cycle. The power delivered is therefore proportional to the number of cycles per unit time i.e. the frequency. Hence, control is provided by maintaining a constant pulse width for the switch on time, and altering the frequency of the total cycle so that the duty cycle is varied. Resonant mode IC's use voltage feedback as the input to a Voltage controlled Oscillator (VCO) which then alters the frequency accordingly to control the output voltage.

In selecting components for the resonant tank there are a few things to note. Clearly the resonant frequency needs to be chosen so that a complete cycle occurs within one cycle of the oscillator frequency and in determining this value, the additional effects of parasitic inductance and capacitance in the circuit should not be neglected.

Another factor is that the peak current in the resonant tank is larger than the output current. To avoid losses in this area, the capacitor C_R should be chosen with a very low equivalent series resistance (ESR)

9.3 Resonant conversion - The future of Power Supply design?

The advantages that resonance mode control brings have made it the choice of many people for the design technique of the future. TI is currently developing a resonant mode controller to complement and extend its range of switching regulators and to support designers who wish to make use of this exciting technique and the benefits it provides.

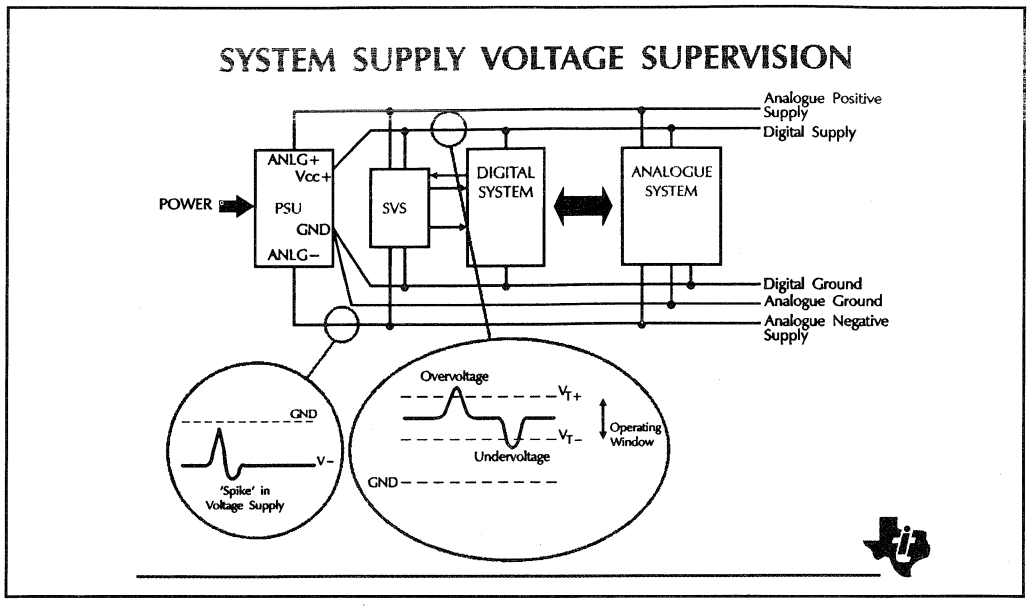


Figure 10 - Supply Voltage Supervision

We have examined in the first section a number of ways to provide a regulated power supply for a system. The methods and devices featured have defined limits of operation and include protection features such as UVLO to ensure reliable operation. Nevertheless, there are still possibilities of fault conditions, such as variations in the supply to the regulator, which cannot be immediately corrected. In these cases, the result is a variation in the regulated supply voltage to the system.

In an analogue system, such variations can cause a degradation of the signal to noise ratio and the dynamic range of the system. However, this will occur as an increase in the level of the noise floor of the system and its effect can therefore be predicted .With a digital system however, the results can be more immediate and dramatic. Since a supply fault can affect any of the digital bits equally, it is just as likely that the MSB will be altered as the LSB , resulting in a possible change of the output by a factor of 2.

The majority of digital systems operate from a 5V supply, used by microprocessors and supporting logic . These devices have a defined operating window , within which they are guaranteed to process data correctly. Incorrect operation can be caused either by ***undervoltage*** when the supply falls below its defined level, or ***overvoltage*** when the supply exceeds its defined level. Undervoltage is the more commen problem since the regulator can normally cope with an increase in its supply, but when the supply falls, the output from the regulator falls with it. It is also good practice to minimise the dropout between the input and output of the regulator to minimise power dissipation. A negative-going spike on the input is therefore transmitted to the output as an undervoltage condition.

The job of a supply voltage supervisor (SVS) is therefore to monitor the supply voltage to a system, and to ensure the system only operates within a defined supply voltage "window" , by applying a reset signal to shut it down when the supply deviates outside this window . A secondary function of the SVS is to ensure the system powers up correctly , by applying the reset to the system until the supply has stabilised. A simple RC network can be used for this purpose but it is subject to noise on the supply and therefore does not provide a clean signal.

Texas Instruments pioneered the monolithic SVS with the introduction of the TL7705A family of devices that provide a reset on an undervoltage condition and a clean power up reset . In addition , they can be used to provide a controlled reset of defined pulse-width to the system to ensure a complete reset.

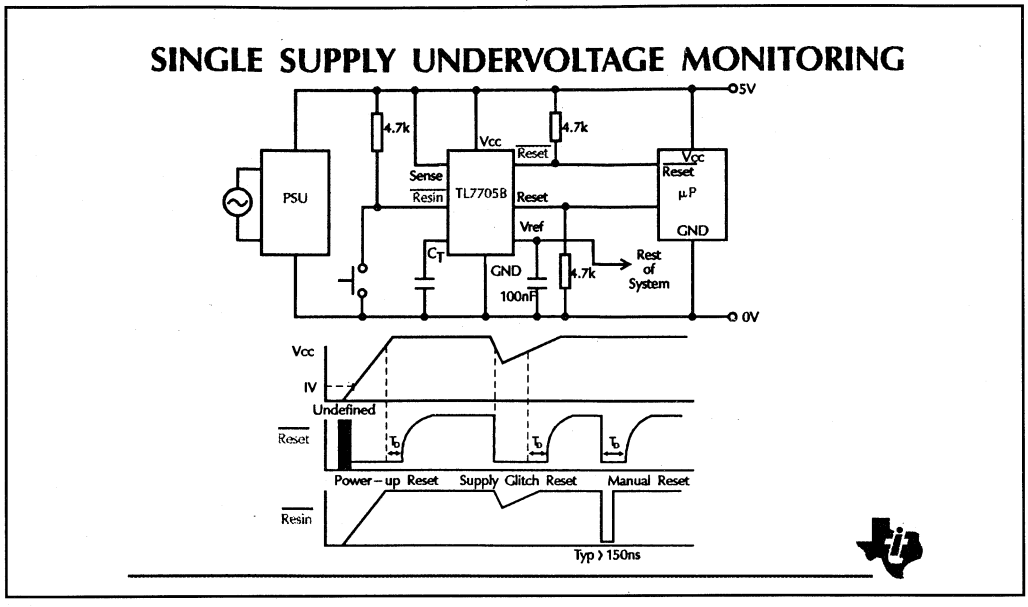


Figure 11 - Single rail Supply Voltage Supervision - The TL7705B

The diagram shows a typical application for supply voltage supervision using the new "B" version of the TL7705. This device is an improved version of the original family bringing two main benefits.

Firstly, the Reset output is defined active low for V_{CC} greater than 1V. This ensures the power up reset is defined before the digital system starts to power up. There are also considerable improvements in the switching speed with the rise and fall time of the reset output greatly reduced. Coupled with shorter propagation delays this gives an improved response rate to a fault condition .

The Reset outputs have complementary positive and negative logic outputs for greater flexibility in interfacing to a number of different microcontrollers. Some microprocessors have I/O ports which not only receive a reset input but also provide a reset output to peripheral devices. If the SVS had active totem pole outputs this could create a situation where the SVS was trying to output a high level signal and the microprocessor was trying to hold the line low, hence creating a short circuit. By having open collector outputs and a pull-up resistor , this situation is avoided. The choice of 4.7kΩ is a compromise between the pull-up speed and the power dissipation.

An external timing capacitor C_T is used to programme a delay time. This holds the Reset in the low (off) state for a fixed time after the sense input has reached the operating threshold and so ensures that the supply is stable before the reset is released. The delay time T_D is defined from the following equation

$$T_D = 1.4 \times 10^3 \times C_T \qquad 11.1.1$$

(for T_D in Seconds and C_T in Farads)

A 2.5V reference output is also provided. It is recommended that this is connected to ground via an external capacitor (typically 0.1μF) to remove high frequency transients from the supply.

TL7705B Single SVS

O Power on Reset generator
O Defined outputs at 1V Vcc
O Precision voltage sensor
O Temperature compensated reference
O Externally adjustable pulse duration

The Resin input allows the user to provide an external reset signal to the system. This is "ORed" together with the sense input internally so that the Reset can be generated from either input. The Resin input can also be used to provide a watchdog function whereby watchdog refresh pulses generated in the microprocessor are integrated by a capacitor to maintain a constant voltage . If the pulses are interrupted, the charge on the capacitor decays and the voltage falls below the threshold, so generating a reset. (Complete details on how to implement the watchdog function are available from TI as an application brief entitled " Microprocessor system fault security)

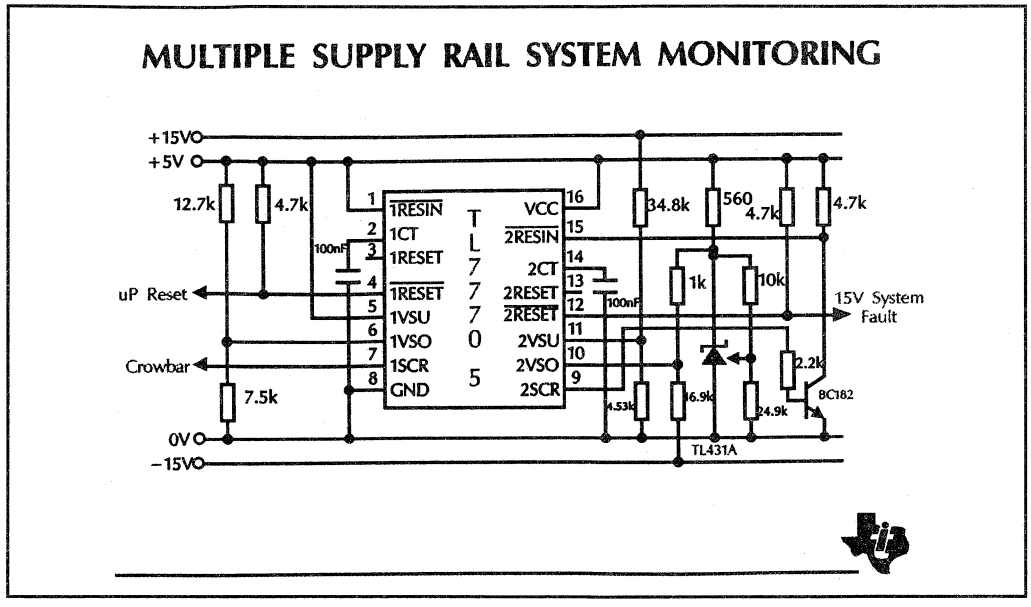


Figure 12 - Multiple rail Supply Voltage Supervision - The TL7770-5

An increasing requirement of many new systems is the ability to monitor multiple supply rails. Typical applications for this include microprocessor systems with associated analogue functions. For example, a system might include a 5V microprocessor outputting data via an RS-232 interface with transceivers operating at +12V and -12V. Alternatively, the data could be passed to a DAC and op amps requiring +/- 15V rails. In each case, it is required to monitor multiple supply rails to ensure each part of the system is operating within its defined limits.

The TL7770-5 family is designed for this purpose. Each member of the family is a dual SVS with inputs to monitor both undervoltage (1VSU and 2VSU) and overvoltage (1VSO and 2VSO) on each of two channels. However, it can be configured to monitor up to four separate rails for undervoltage if so required.

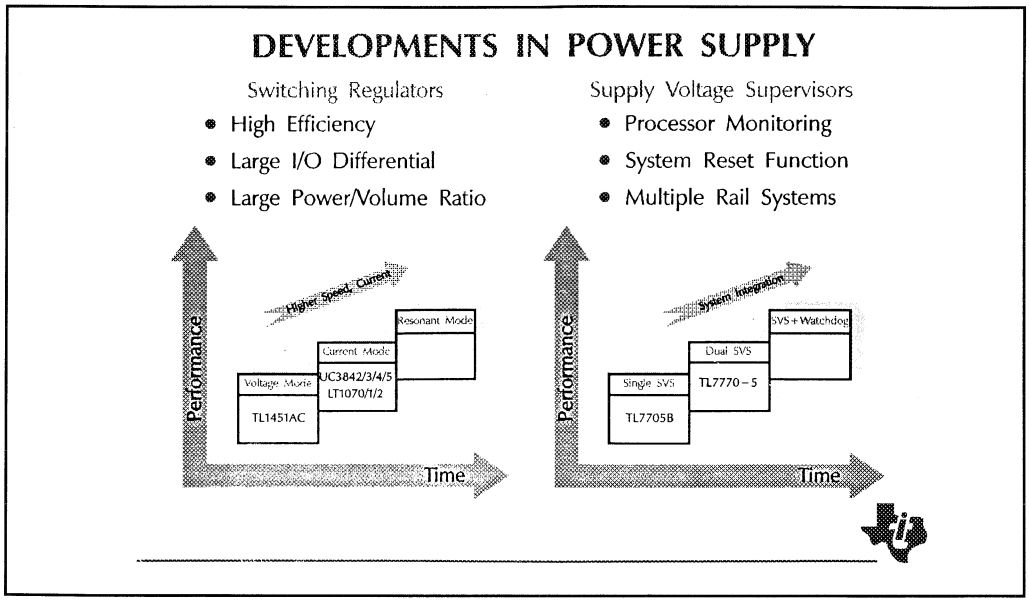
TL7770-5 Dual SVS

O Power on Reset generator
O Wide supply voltage range 3.5V to 18V
O Defined outputs at 1V Vcc
O 250mA SCR drive outputs
O Precision Overvoltage and Undervoltage sensors
O Temperature compensated reference
O Externally adjustable pulse duration

The diagram shows a typical application monitoring both under and overvoltage on a 5V rail, and undervoltage on the +/-15V rails. On each member of the family except the TL7770-2, the 1VSU input is defined to sense a specified threshold voltage by an internal potential divider. For the other sense inputs, this threshold can be programmed by using an external divider. For example, at the 1VSO input, the divider is set so that the voltage is 2.6V when the input on the V_{CC} rail is 7V. This is the internal threshold of the VSO inputs. If V_{CC} gets any higher, the 1SCR output is turned on. Here it provides the gate drive for an SCR , so that the

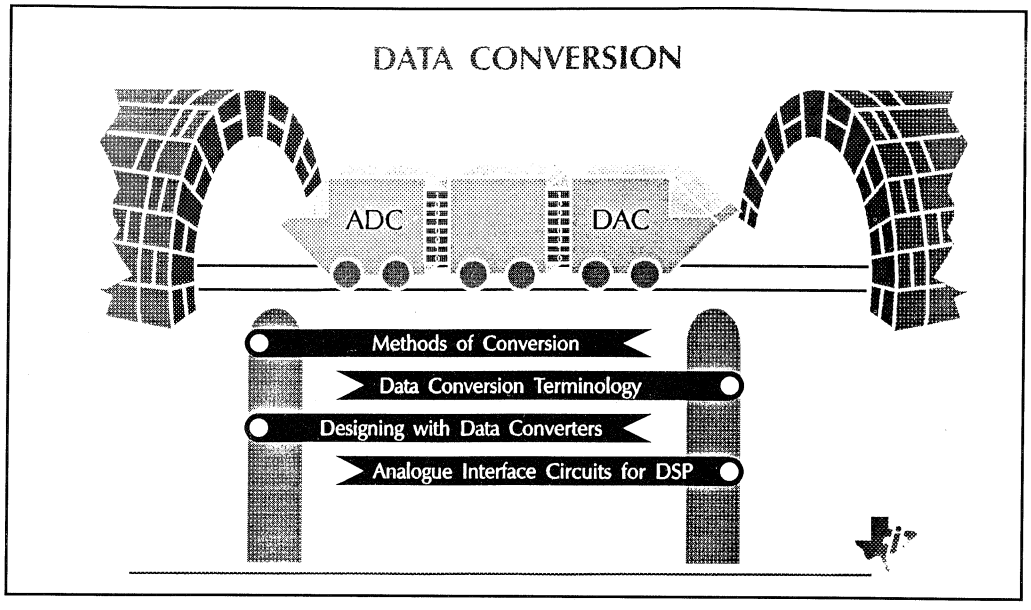
supply rail is made short circuit to ground. This will blow the protection fuse and shut down the system using the "crowbar" technique.

This application also shows how the VSO inputs can be used to montor undervoltage. A resistor network connects the -15V supply to a 4V reference generated by the TL431A. The use of the reference rather than the 5V supply rail eliminates the effects of variations in that supply. The values are chosen to set a value of 2.6V at 2VSO when the supply reaches -13V. If it falls further, the value at 2VSO will rise above 2.6V and trigger the 2SCR output. This time, the drive is used to turn on a 2N2222 transistor, which in turn pulls the 2 Resin input low . This will activate the 2 Reset output.



SECTION 3.
DATA CONVERSION

DATA CONVERSION INDEX



Section 1 : Methods of conversion

This first section looks at the methods used to "translate" between the analog and the digital worlds. It explains the advantages and disadvantages of each type, and what makes it the appropriate choice for a particular application.

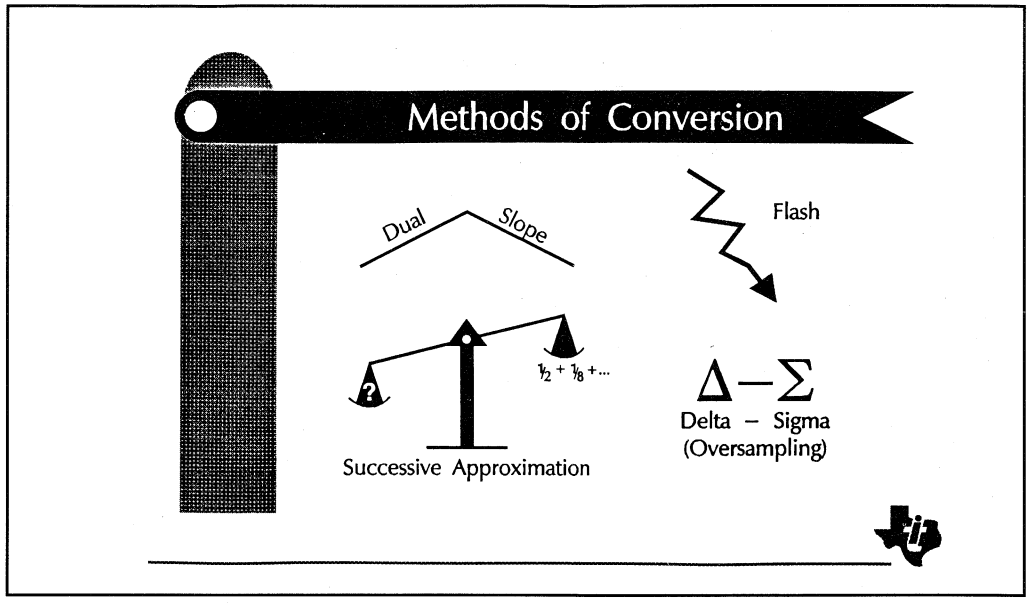


Figure 1 - Methods of conversion

Data acquisition is the process of transforming analogue electrical signals into digital information for storage, display, processing, data transmission or control. A data acquisition system is an electronic system used to perform this task and comprises sensors, transducers, signal conditioning, sample and hold circuits, analogue multiplexers, and analogue to digital converters (ADC). Recovery of a digital signal into analogue form is sometimes required. The components, such as digital to analogue converters (DAC) and filters, used to perform this function are also covered under the heading of data conversion.

Applications for data acquisition systems cover a wide range; from weighscales, speech and audio processing to instrumentation and video recorders. Each application has its own requirements but two common parameters must be considered in all systems. These are ***bits of resolution***, and ***conversion time***. To meet these diverse needs , different conversion methods are employed. Some are optimised for speed of conversion, while others are known for their higher resolution. Six common techniques for analogue to digital (A/D) conversion are as follows:

- O Single Slope
- O Dual Slope
- O Successive Approximation
- O Semi-Flash
- O Flash
- O Oversampling (Delta-Sigma)

Conversion methods for digital to analogue (D/A) signal recovery also vary with the speed and resolution requirements. In the following examples, some of the common conversion techniques will be discussed and related to typical applications.

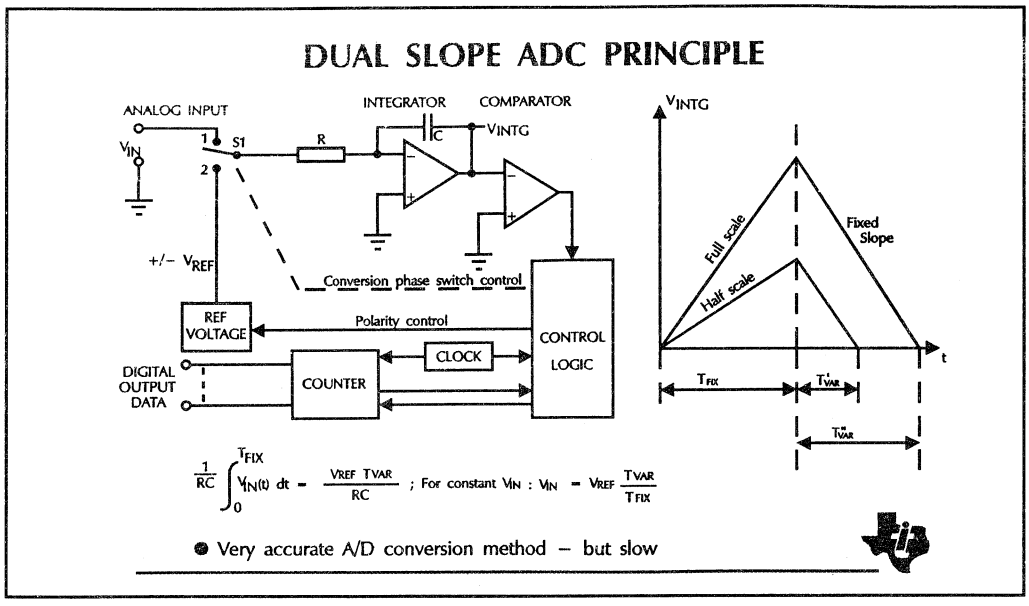


Figure 2 - Dual slope principle

The most simple A/D conversion method is the Single-Slope technique, which arrives at its digital output by comparing the unknown analogue input signal with a ramp voltage. A digital value is obtained by counting the number of clock pulses needed to build a ramp from 0V to the value of the unknown analogue input signal. The requirements for a good single slope converter are a stable reference voltage, clock, ramp generator and low offset comparator. Integrated implementations are usually low to medium accuracy. This technique however has a long conversion time .

Dual Slope conversion is also slow but very accurate. The method uses a counter and an integrator to convert an unknown analogue input voltage into a ratio of time periods multiplied by a reference voltage. A first integration is over a fixed period of time, T_{FIX}, and uses an unknown analogue voltage, V_{IN} as input. At the end of the integration period , a peak value proportional to the input voltage is held on the integrator output. S1 is then switched to position 2 and a second integration period takes place. This uses a reference voltage, V_{REF} of opposite polarity , which is used as the input to the integrator whose output ramps down at a rate only dependent on the reference value. The resultant value of the first period is integrated down to 0V in a variable time, T_{VAR} proportional to the amplitude of the input signal, V_{IN}.

Putting these two ramps together, using the same clock to count time periods T_{FIX} and T_{VAR}, the unknown input voltage V_{IN} can be determined from:

$$V_{IN} = V_{REF} \times (T_{VAR} / T_{FIX}) \qquad 2.1.1$$

Using the same integrating network cancels errors due to comparator offset, capacitor tolerances, long term counter clock drift and integrator nonlinearities.

While the conversion speed of a dual slope converter is slow (milliseconds), high resolution (10-16 bits) is possible. Resolution is determined from the ratio of counts in the integration periods. For example 1 in 20,000 counts is equivalent to better than 14 bits of resolution, with the basic error as +/-1 count plus the reference voltage error.

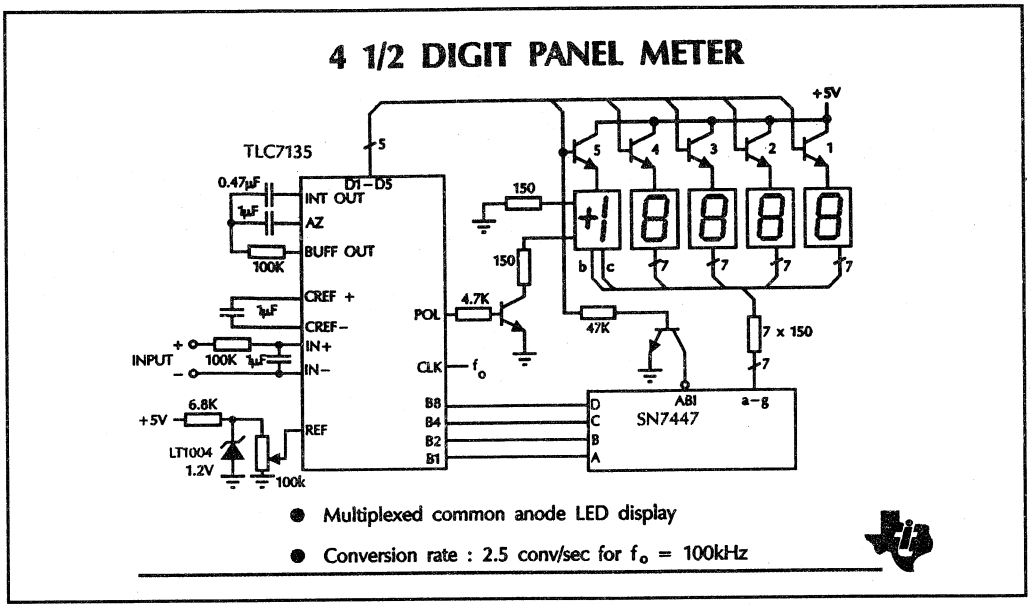


Figure 3 - 4 1/2 Digit panel meter using TLC7135

Dual slope converters such as the LinCMOS(TM) TLC7135 are ideally suited to any application which requires precise measurement of slowly varying analogue signals. The TLC7135 offers resolution of 50 ppm (one part in 20,000) making it an excellent choice for applications such as digital voltmeters, precision panel meters, weigh-scales and for precise or wide-range temperature measurement with a visual display.

In this general purpose 41/2 digit panel meter, a voltage input or transducer signal (transformed into a voltage between +/-2V) is converted with more than 14 bits resolution. The result is displayed including sign on a 41/2 digit LED display. The TLC7135 has multiplexed binary coded decimal outputs which are easily interfaced to many numeric displays. The common-anode driver in this application (transistor array 1-5) drives the digit indicated by the digit select lines (D1-D5). The binary coded decimal (BCD) to seven segment decoder "SN7447" determines which segments of the LED are lit to form the correct digit. The most significant digit is blanked on zero reading.

TLC7135

- **O 4 1/2 digit precision ADC**
- **O 50ppm resolution**
- **O 1pA typical input current**
- **O Zero error < 10μV**
- **O Autoranging capability**
- **O Easy interface to uP and UARTs**
- **O Multiplexed BCD output**

The circuit uses a low power LT1004 1.2V bandgap reference available from Texas Instruments. The input shows a typical RC filter for input signal smoothing. Depending on the

needs of the application, the time constant for this filter can be made shorter or longer, or the filter can be deleted completely if not required. The 0.47µF integrating capacitor should be of a type with low dielectric absorption such as a polypropylene capacitor. However, polystyrene or polycarbonate capacitors will also work well. A high dielectric absorption causes the integrating capacitor value to be different during the integrate and de-integrate phases. Choosing the clock frequency f_O, such that an integral multiple of 50Hz periods occur during the signal integrate phase, maximizes the 50Hz pick-up rejection. The applied f_O=100kHz is such a frequency providing 2.5 conversions per second.

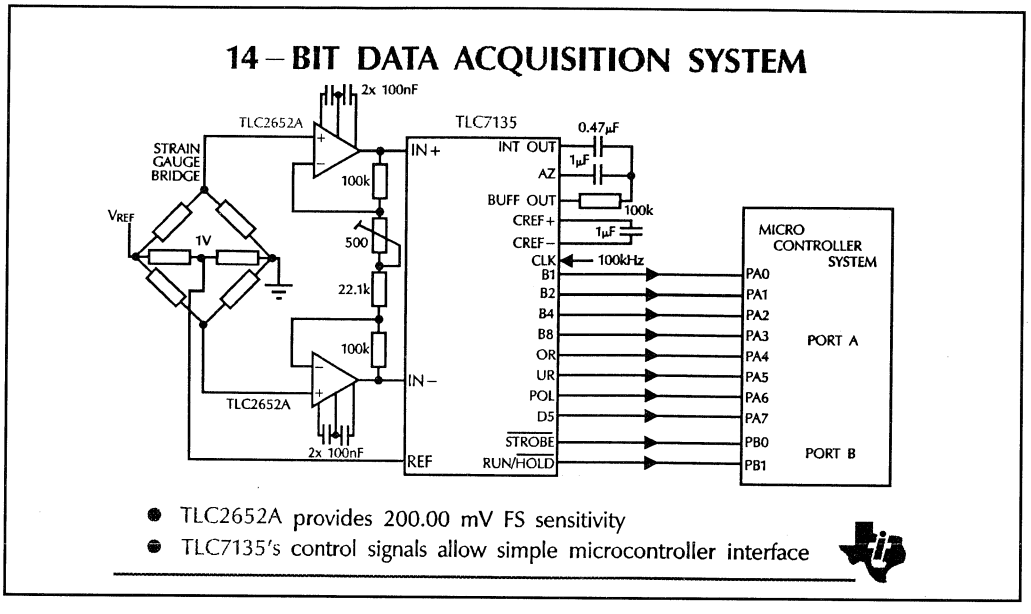


Figure 4 - A 14 bit data acquisition system

The TLC7135 interfaces easily to UARTs or microprocessor systems via control signals. The control lines BUSY, STROBE, RUN/HOLD, OVER-RANGE and UNDER-RANGE support microprocessor based measurement systems. The control signals can also support remote data acquisition systems with data transfer via universal asynchronous receiver transmitters (UARTs).

In this application only 10 interface lines are required for the interface between the 14 bit accurate converter and a microprocessor or peripheral parallel port. It is possible to eliminate the use of the multiplexed digit select lines (D1-D4) by counting the digit strobes from the STROBE output in a software register. The most significant digit select line (D5) is used to simply monitor that an end-of-conversion has occurred.

In order to synchronize data transfer between microprocessor and TLC7135, the microprocessor tests D5. If D5 is true, then an end-of-conversion has occurred. A data pointer is then initialized and assembly of five BCD coded digits begins. The next four STROBE pulses will find D5 false, causing the BCD digits to be stored in memory or register locations. The fifth STROBE pulse signals an end of data transfer, so the user can display or manipulate the data as desired. The RUN/HOLD input allows the microprocessor to control the TLC7135 mode of operation. Holding RUN/HOLD high results in continous conversions. When RUN/HOLD is held low the TLC7135 will remain in auto-zero mode. If RUN/HOLD is pulsed high, the TLC7135 will perform a conversion, output new data, and return to auto-zero mode.

The TLC7135 has a standard +/-2V full scale input voltage and 20,000 counts maximum; e.g. one count corresponds to 100µV. Additionally, its analogue zero error is less than 10µV and the drift less than 0.5µV/ °C. Consequently, if increased sensitivity is required, extreme DC precision op amps are required for amplification.

In this application the sensitivity has been increased by a factor of ten to 200mV for full scale without compromising accuracy. Two TLC2652A chopper-stabilized op amps with a maximum of 1µV offset voltage and negligible drift amplify the strain-gauge bridge signal 10 times using an instrumentation amplifier configuration. 1 count in this application corresponds to only 10µV strain-gauge bridge signal.

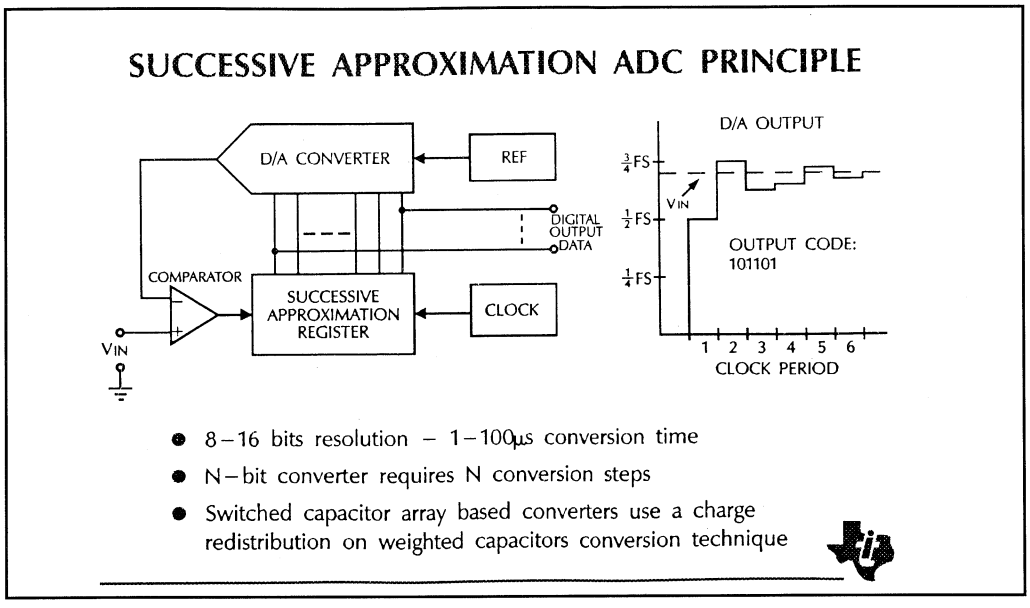


Figure 5 - Successive approximation

Successive approximation ADCs continue to be the most popular type of converter. A wide range of devices with resolution from 8-16 bits are available and with conversion rates from 100µs to below 1µs. Successive comparison of an unknown analogue input voltage with binary weighted values of a reference give this method its name of "successive approximation". A converter of N-bit resolution takes "N" steps to achieve a digital output.

One input of the comparator, shown in the block diagram, is driven by an unknown input signal, V_{IN}, while the output of the DAC drives the other. The successive approximation register provides the input to the DAC and responds to the output from the comparator.

When the DAC has its MSB set to logic 1 (with all other bits zero), by the successive approximation register (SAR), it will produce a voltage output of 1/2 the reference and analogue input full scale range. The comparator then determines if the DAC output is above or below the unknown input signal. If, as shown, the input signal V_{IN} is above the DAC output value, the MSB is retained in the successive approximation register while the next weight of 1/4 the reference is compared. This process continues until all bits are tested and the nearest approximation to the input signal is obtained. The result is then passed to the output register.

While the successive approximation converter process continues, the input signal must be held constant using a sample and hold circuit in front of the comparator. Alternatively, the signal should, as a rule of thumb, vary maximum 1/2 LSB during conversion. This puts a

slew-rate or full scale frequency limitation on the signals the converter can handle.

More recent successive approximation converter designs, using switched capacitor networks utilizing charge redistribution, are replacing older designs using resistive ladder DACs. This is due to the switched capacitor technique's smaller chip area, higher speed and inherent sample and hold function. Texas Instrument's Advanced LinCMOS technology with its double polysilicon layers is an ideal process for building well matched switched capacitor circuits for successive approximation ADCs.

A wide range of 8-10 bit LinCMOS successive approximation ADCs with serial or parallel output and input multiplexer options are available from Texas Instruments. Please consult the data book for further information.

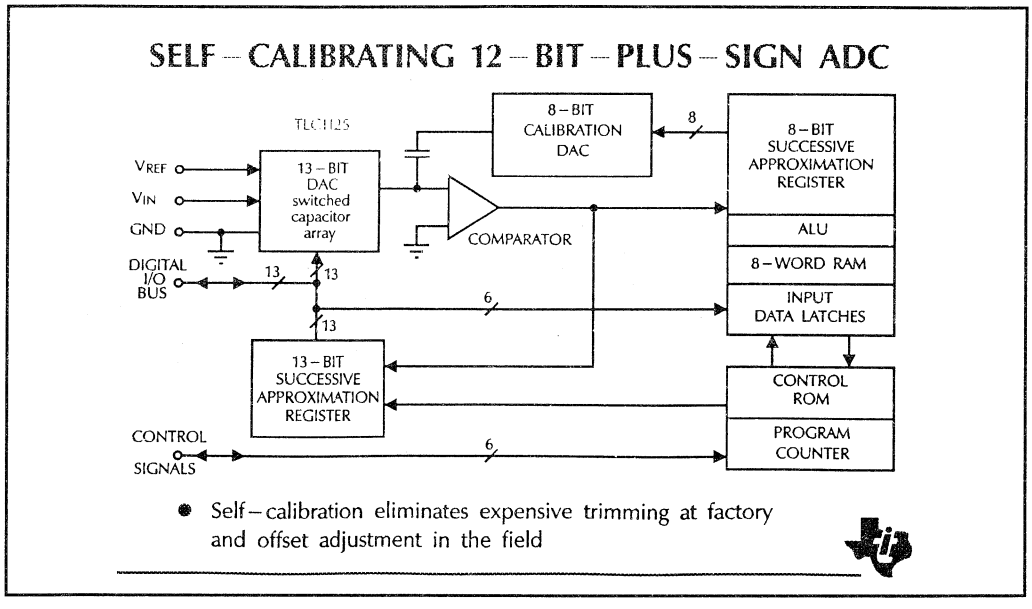


Figure 6 - Self calibrating 12 bit plus sign ADC - The TLC1125

TLC1125 is a 12-bit-plus-sign successive approximation ADC utilizing a self-calibration technique to eliminate expensive trimming of thin-film resistors at the factory. Additionally, this technique ensures excellent long term stability, avoiding regular field trimming to maintain conversion accuracy.

The design uses a switched capacitor based charge redistribution technique for the D/A conversion. As 12-13 bits accuracy of capacitor matching is difficult to achieve, seven of them are calibrated during a non-conversion, capacitor-calibrate cycle in which all seven of the capacitors are calibrated at the same time. The calibration or conversion cycle may be initiated at any time by issuing the proper command word to the data bus.

TLC1125 Self calibrating ADC

O Self calibration eliminates expensive trimming
O 0V to 5V Unipolar or -5V to +5V Bipolar ranges
O 12μS conversion time
O True differential inputs
O Low Power . . . 85mW max

6.1 Calibration cycle (simplified description)

6.1.1 Comparator Offset Calibration Steps:

Step 1 : The input, V_{IN} is shorted to GND in order to ensure that the comparator input is zero. A coarse offset calibration is performed by manipulating the offset error using switches and offset storage capacitors. After this action some of the offset still remains uncalibrated.
Step 2 : An A/D conversion is done on the remaining comparator offset with the 8 bit calibration DAC and 8 bit successive approximation register. The result is stored in the RAM.

6.1.2 13 Bit DAC Capacitive Ladder Calibration Steps:

Step 1 : The input is internally disconnected from the 13 bit capacitive DAC.
Step 2 : The MSB capacitor is tied to V_{REF}, while the rest of the ladder capacitors are tied to GND. The ADC conversion result from the Comparator Offset Calibration Step 2 above, is retrieved from the RAM and is input to the 8 bit DAC.
Step 3 : Step 1 of the Comparator Offset Calibration sequence is performed. The 8 bit DAC input is returned to zero and the remaining comparator offset is then subtracted. Thus, the comparator offset is completely corrected.
Step 4 : Now the MSB capacitor is tied to GND, while the rest of the capacitors are tied to V_{REF}. An MSB capacitor voltage error on the comparator output will occur if the MSB capacitor does not equal the sum of the other capacitors in the capacitive ladder. This error voltage is converted to an 8 bit word and stored in the RAM.
Step 5 : The capacitor voltage error for the next most significant capacitor is calibrated by keeping the MSB capacitor grounded and then performing the above Step 1-4 while using the next most significant capacitor in lieu of the MSB capacitor. The seven most significant capacitors can be calibrated in this manner.

6.2 Conversion Cycle (simplified description)

Step 1 : Step 1 of the Comparator Offset Calibration sequence is performed. The remaining offset obtained in Step 2 of the Comparator Calibration sequence, is retrieved from the RAM and is input to the 8 bit DAC. Thus, the comparator offset is completely corrected.
Step 2 : The input signal, V_{IN} is sampled onto the 13 bit capacitive ladder.
Step 3 : The 13 bit ADC conversion is performed. As the successive approximation conversion proceeds successively through the seven most significant capacitors, the error for each of these capacitors is recovered from the RAM and accumulated in the 8 bit successive approximation register. This register controls the 8 bit DAC so the total accumulated error for these capacitors is subtracted out during the conversion process.

A conversion takes only 12μs. A calibration cycle takes 4 times longer. Calibration is required upon power-up to achieve full accuracy. Regular recalibration is recommended to avoid drift. This is particularly true in systems where self-heating or environmental temperature changes occur.

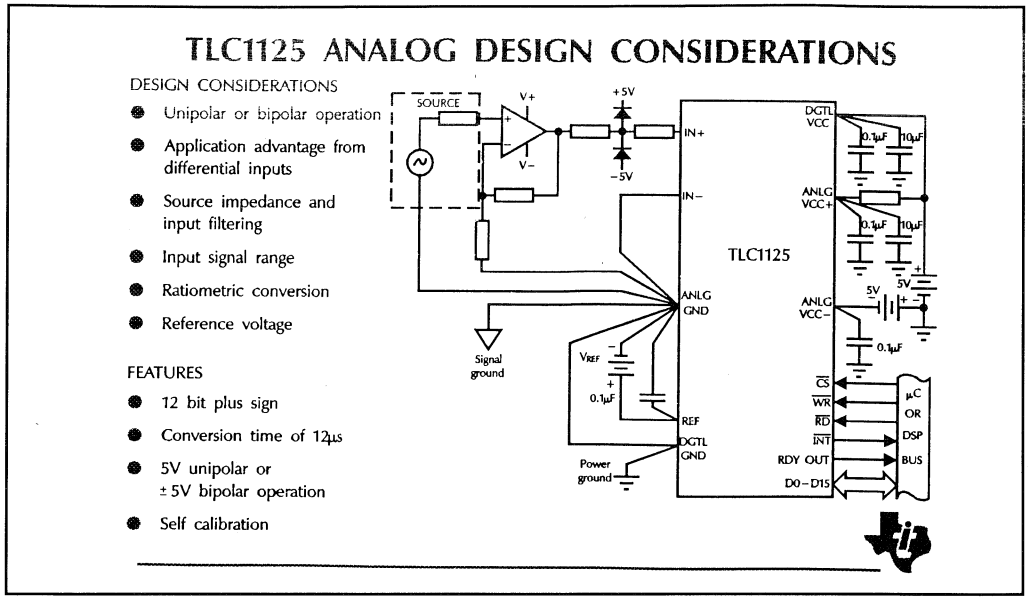


Figure 7 - TLC1125 Analogue design considerations

When designing with a medium to high resolution converter like the TLC1125 several fundamental considerations have to be made.

7.1. Power supply

The device features a 0 to 5V analogue input range with a single +5V supply voltage (Unipolar configuration) or -5 to +5V analogue input range with +/-5V supplies (Bipolar configuration). The choice of the configuration depends on the application and available supply voltages.

Proper supply grounding of both digital and analogue supplies are required as shown. Avoid ground loops that inductively could pick up hum. Also, signal ground leads should only carry the return current from the signal source. Any additional current may cause a voltage drop and result in system errors. Noise spikes on the supply lines can also cause conversion errors.

All supply input pins should be bypassed by 1 to 10µF low inductance tantalum capacitors with short leads. Further high frequency decoupling can be achieved with a 100nF ceramic capacitor, placed in parallel with the aforementioned tantalum capacitors. A separate regulator for the TLC1125 or other analogue circuitry will greatly reduce digital noise on the analogue supply line.

7.2. Differential inputs

The device is provided with a true differential input structure. This can be utilized to reduce effects of noise and hum signals common to both input wires. Common-mode noise often appears where long input leads are used or in noisy environments. There is no time interval between the sampling of IN+ and IN- input so these are truly differential and simultaneous sampling rejects even high frequency common-mode signals within the bandwidth of the ADC. Keep IN+ and IN- input leads twisted and their PCB tracks close together.

The true differential input structure allows for simple interface to differential sources such as some strain-gauge configurations. Also, the input can often save a pre-processing differential instrumentation amplifier or act as the third amplifier in such a configuration.

7.3. Noise constraints

A general rule of thumb is that the input leads should be kept as short as possible and that the source impedance should be as low as possible.

Long input leads can pick up noise from a digital clock signal with edges too fast for the differential input amplifier's common-mode rejection. This noise can cause conversion errors.

Input bypass capacitors may be used for noise filtering. However, the charge on these capacitors will be depleted during the input sampling process when the internal sampling capacitors are charged. Note that the charging of the bypass capacitors through the differential source impedance must keep pace with the charge depletion of the bypass capacitors during the sampling sequence. The above phenomenon becomes more significant as source impedance and conversion rate increases. For source impedances below 100 Ohm, a 1nF bypass capacitor at the input will prevent pick-up due to series lead inductance of a long wire.

Even in applications without an input bypass filter capacitor, high source impedance can cause a voltage drop when charging the internal capacitors during the sampling phase. Note, that some op amps, when used as signal source, have high output impedance for the current spikes required to charge the internal capacitors of the TLC1125.

7.4. Signal conditioning

The input signal range is limited by the supply voltages which means 0 to 5V in unipolar mode and -5 to +5V in bipolar mode of operation.

In either mode, when using a signal conditioning op amp supplied from the same analogue supply (supplies), you will need an output swing to the supply rails within a fraction of a millivolt. No op amp can guarantee this performance but some come very close. The LinCMOS precision op amp TLC2201 has a complementary CMOS output state that can swing very close to either rail when not loaded. In addition, it can operate with a single +5V supply as well as with +/-5V supplies. Using this op amp eliminates adjustment of the input range, but a few codes in both the top and bottom of the ADCs dynamic range will be missed due to the limited output swing. A worse limitation is often the accuracy and stability of the power supply (supplies) limiting the input range significantly, even if 1% voltage regulators are used.

For applications demanding high frequency signal conditioning a faster precision op amp like the TLC2027/37 should be employed. However, such op amps have not got rail-to-rail output swing so higher supply voltages must be used. If +V and -V exceeds the ADC supplies, precautions must be taken to avoid over-voltage on the ADC's input pins. A suitable protection can be accomplished by a small series resistor (preferable a PTC resistor) followed by schottky clamping diodes to either supply. To ensure that the bulk of current from any over-voltage will flow in the schottky diodes rather than in the ADC's internal ESD protection circuitry, an additional small series resistor can be added in series with the input. The maximum input current for the ADC caused by over-voltage should be kept well below +/-5mA.

7.5. Mode of operation

The ADC can be used in either absolute or ratiometric reference applications. In an absolute reference system, where the analogue input varies between very specific voltage limits, a 12-13

bit precision voltage source reference is required. An example of such an application is a temperature measuring system using a sensor, which provides 10mV/°C independent of the supply voltage.

In a ratiometric system, the analogue input voltage is proportional to the voltage used for the A/D reference. When this voltage is the system power supply, the REF pin can be tied to the ADC's positive supply. This technique relaxes the stability requirement of the system reference as the analogue input and the ADC reference move together maintaining the same output code for a given input condition. An example of a ratiometric transducer is a strain-gauge bridge supplied directly from the system power supply. Often both the VIN- and the REF pins are tied to the system power supply via resistive voltage dividers to define an input dynamic range window slightly smaller than that of the supply voltages. This allows a driving op amp to operate at the same supplies as the ADC without needing rail-to-rail swing.

7.6. Reference input

The restrictions on the source impedance for the analogue inputs also applies to the reference input. In addition, noise from the reference must be kept at a minimum by careful decoupling of both low and high frequency noise.

In summary, precision 12 bit ADCs require some adjustments to compensate for offset errors. The TLC1125, with its self-calibration facility ensures low and stable offset with time and temperature eliminating initial trimming and re-adjustment due to aging.

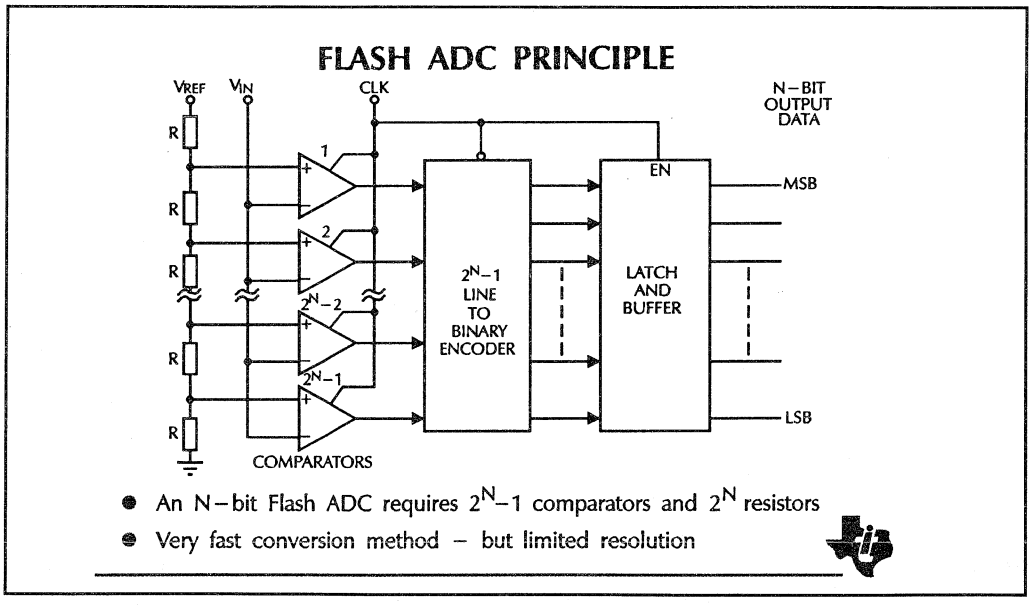


Figure 8 - Flash Analogue to digital conversion

The flash ADC derives its name from its ability to do a very fast conversion. This is accomplished by providing a comparator for every quantisation level. Hence, an N bit flash ADC requires 2^N - 1 comparators.

These comparators all examine the input simultaneously and make an immediate conversion. The block diagram shows that each comparator has one input connected to the input signal and the other to a tap on a reference potential divider. The resultant so-called

"thermometer" code is then encoded into binary and is output through a latch. This technique provides the fastest means of conversion but requires the use of a large die area for the comparators and resistor ladder .

Presently, the flash converters available cover 4-10 bit resolution with sampling rates into the Gigaherz range. However, the most popular applications are in the video field, where 6-8 bit resolution and 20 mega samples per second are the standard specifications.

A compromise between "speed" and chip area is the semiflash method using a two step flash principle. In this case, the most significant bits are coded first and then the remaining bits afterwards. This trades off a reduction in speed with a reduction in the number of comparators required and consequently the size (and cost) of the die. An example is the LinCMOS 8 bit semiflash ADC, TLC0820 with a conversion rate up to approximately 1 mega-samples per second.

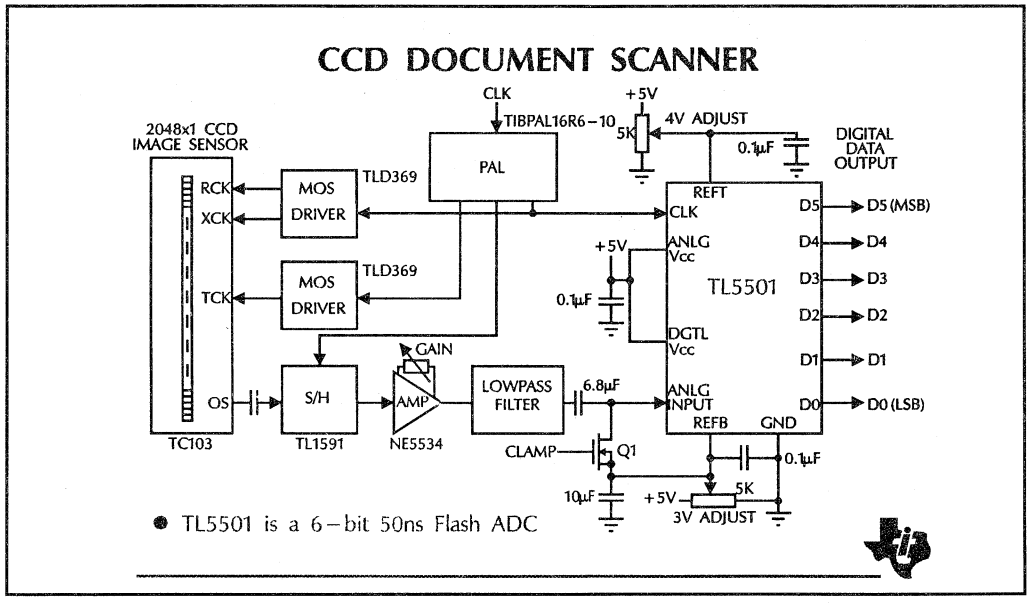


Figure 9 - CCD Document scanner

Document scanners for facsimile transmission (FAX machines) over the public telephone network are an expanding market.

TL5501 Flash ADC

- **O 6 bit resolution**
- **O 1/2 LSB linearity**
- **O Conversion rate up to 20MSPS**
- **O Analogue input range ...1V**
- **O 5V single supply operation**

This implementation is scanning the document using a TC103 (2048 x 1) CCD line image sensor controlled from a PAL chip via some TLD369 MOS drivers and level shifters. The CCD output video signal data stream (typ 500kHz) is superimposed on a DC voltage and reset between each pixel. A coupling capacitor removes the DC and a TL1591 sample and hold

circuit holds the signal level between pixels leaving a continous video envelope. The video signal is then amplified to a one volt peak to peak signal required by the TL5501 flash ADC. Post lowpass filtering removes residual clock signals. The video signal is then clamped to +3V by Q1 to provide DC restoration and adjust the DC component for the ADC input pin ANLG INPUT. The digitized video signal appears at a pixel rate of typically 500kHz on the output of the TL5501 ADC.

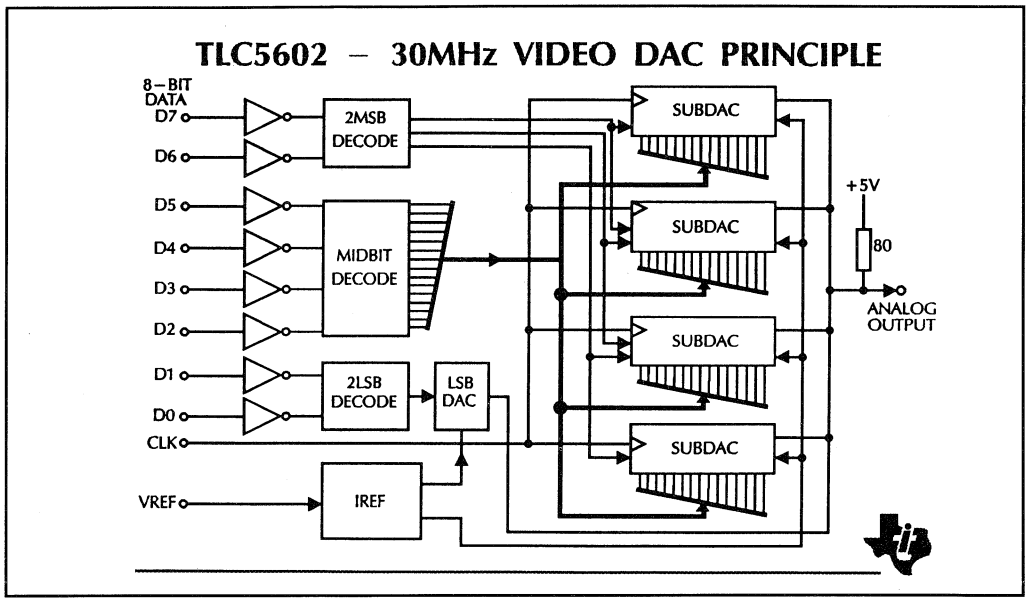


Figure 10 -TLC5602 : A 30 MHz Video DAC

A traditional problem with high speed DACs is that of glitch errors which occur at the changeover from one code to the next. This is especially true at the midpoint code where all bits change at the same time. If there are differences in internal propagation delays, there can be large transient errors at the output as the bits change over.
To overcome this problem the 8 bit TLC5602 DAC is designed with three distinct building blocks.

1. The two least significant bits determination block
2. The two most significant bits determination and control block
3. The four middle bits determination block

The whole DAC works on the basis of summation of current, which is controlled by the I_{REF} block. As the digital input code increases, the amount of current drawn is reduced, so that the output voltage increases linearly.

The input binary word is divided into three. The middle four bits (D2-D6) are fed to a decoder which controls a series of FET switches . For example, if the input were $1010_2 = 10_{10}$, 10 of the switches would be turned off. This code is fed via a bus to four SUBDAC blocks in parallel. The two MSBs then determine which blocks are either fully on, fully off or are responding to the code fed in from the MIDBIT bus. For example, if the MSBs are 01, the first SUBDAC is fully on and the second is controlled by the bus.

The outputs from the SUBDACs are linked at the output where they are summed and converted to a voltage by an internal 80 ohm pull-up resistor.The two least significant bits are determined in a similar manner but switch a smaller ratioed current.

TLC5602 Flash DAC

O 8 bit resolution
O 1/2 LSB linearity
O Conversion rate up to 20MSPS
O Analogue input range ...1V
O 5V single supply operation
O LinEPIC process
O Low Power ... 80mW

This conversion technique has two major advantages:

1. Glitches are greatly reduced because there are only small changes between adjacent codes.
2. Breaking down the mid four bits and using the MSBs as control bits means that similar , small currents are being switched on and off as the digital code increases. Since the SUBDACs are very well matched this provides inherent linearity and means that differential gain errors are much reduced due to code widths being much the same throughout the transfer curve.

The currents are generated using the precise resistance of MOSFETs which are well matched across the whole chip. Additionally, the 1μm LinEPIC CMOS process gives very low power consumption without large glitches on the supply rails.

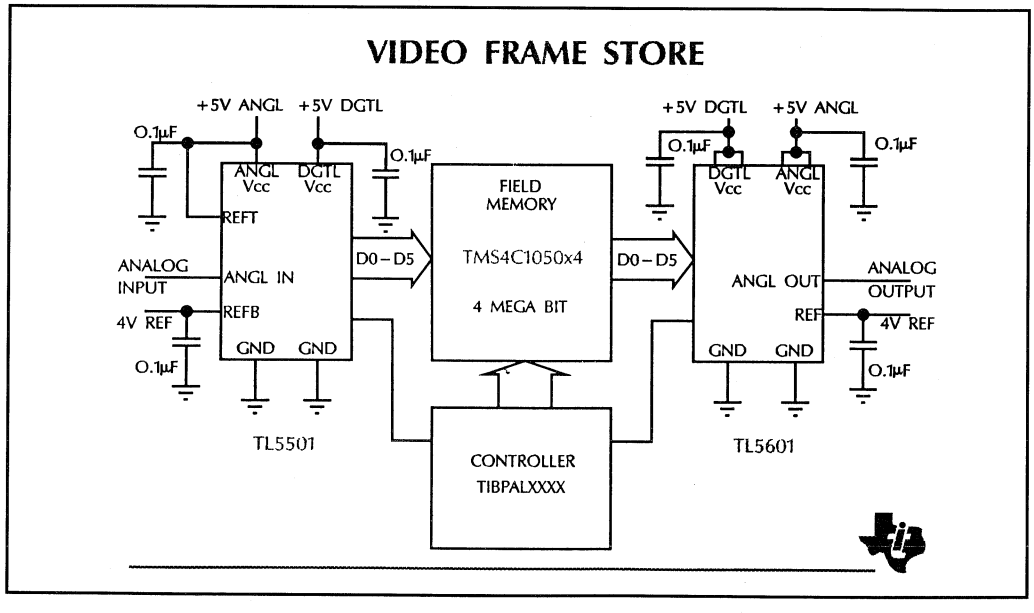


Figure 10.1 A video frame store

A typical application area for 6-8 bit video DACs and flash ADCs is for video recorder frame-store where a video signal frame can be digitized and held in a field memory. By continuous scanning of the stored video picture in the memory followed by digital to analogue conversion a frozen or still video picture is achieved.

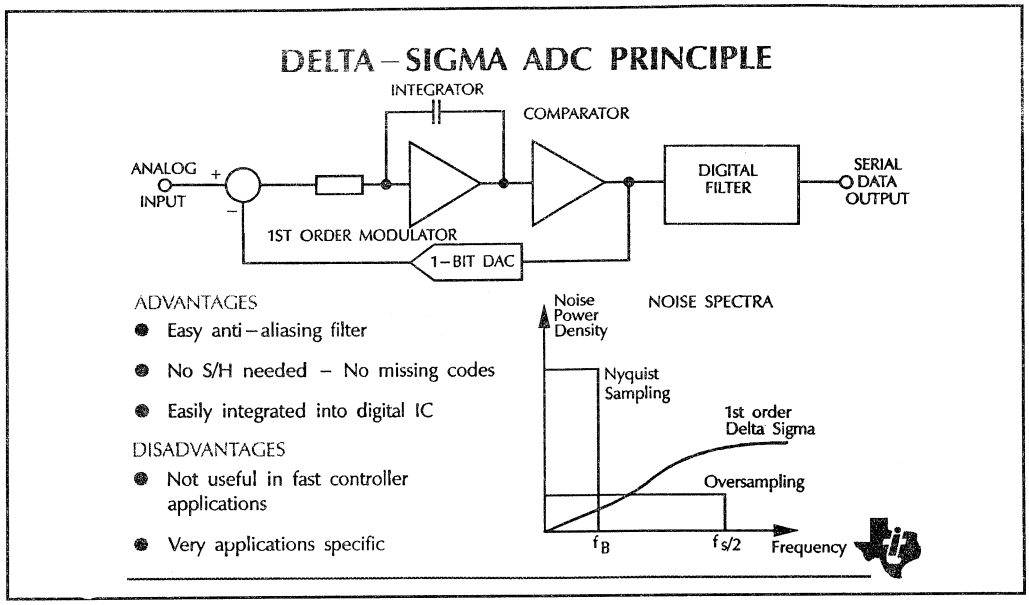


Figure 11 - Delta-Sigma (Δ-Σ) conversion

New analogue to digital converters utilizing the delta-sigma conversion technique have appeared recently. These products are notable not only for their impressive specifications (12-20 bit resolution), but also because they provide a stronger link to the digital IC realm and especially to digital signal processing (DSP). Because of this digital tie-in, the delta-sigma technique is being touted as the preferred replacement (up to a few 100kHz) for all non-video converters.

The basic principle is not new but silicon realizations first started to be cost-competitive with the advent of 1-2μm technologies due to the huge chip area occupied by the required post digital filter. Further reduction in semiconductor geometries below 1μm will make this type of converter even more attractive.

11.1 Delta-Sigma structure

The basic 1st order delta-sigma converter contains two major blocks; a closed-loop integrating modulator and a digital filter. The modulator as shown, consists essentially of a 1 bit DAC, a difference node (hence delta), an analogue integrator (hence sigma), and a clocked comparator. Practical converters have more stages, thus 2nd or 3rd order modulators.

Input signals are digitized on the comparator output and a bit stream is fed to the digital filter and to the 1 bit DAC. The output of the DAC which is controlled from a precision reference is summed at the difference node with the input signal. The job of the signal from the 1 bit DAC - a train of positive or negative constant width, constant amplitude pulses - is to keep the charge on the integrating capacitor, as close to zero as possible. This is accomplished by balancing or nulling the charge.

A positive voltage applied to the input of the modulator begins to appear as charge on the integrator's capacitor and a voltage at its output. The voltage is sensed by the comparator, producing a train of ones at its output and a train of pulses of opposite polarity to the integrator input voltage, through the 1 bit DAC and summing node. When the pulses from the 1 bit DAC have reduced the charge to zero and begin charging it to the opposite polarity, the comparator

will see a negative voltage and produce zeros. The more positive the input voltage, the greater ratio of ones to zeros in the output bit stream. The more negative the input, the greater the ratio of zeros to ones. If the analogue input voltage is zero, an equal number of ones and zeros appear in the output.

To get from the one-bit stream of data coming out of the comparator to a data stream with usable N bit information (for an N bit converter) requires digital signal processing. The digital filter then decimates the single bit stream into words of length N bits.

11.2 The benefit of oversampling

How can a 1 bit ADC give a high S/N ratio? Sampling with a conventional converter at the Nyquest rate places all the quantization noise within the band of interest. Oversampling spreads the quantization noise over a much wider bandwidth reducing the level of noise in the band of interest. Delta-sigma oversampling further reduces the noise in the bandwidth of interest with the noise shaping of the integrator-loop. However, a sharp roll-off digital post filter is required which basically replaces the analogue anti-aliasing input filter required for successive approximation converter types . Delta-sigma converters require only a simple RC filter on the input for anti-aliasing due to a high ratio between the sampling frequency and the maximum frequency of interest.

Although delta-sigma converters are easier to integrate onto digital processes than conventional successive approximation converters which require an anti-aliasing filter, good linear processes are still required for optimum performance of the modulator portion. This design is associated with the usual analogue design requirements including high performance op amps and comparators, matched and voltage insensitive capacitors used for switched capacitor realization of the integrators and finally a precision reference.

Areas where oversampling technique seems especially attractive are speech processing in telecom, audio processing and metering applications.

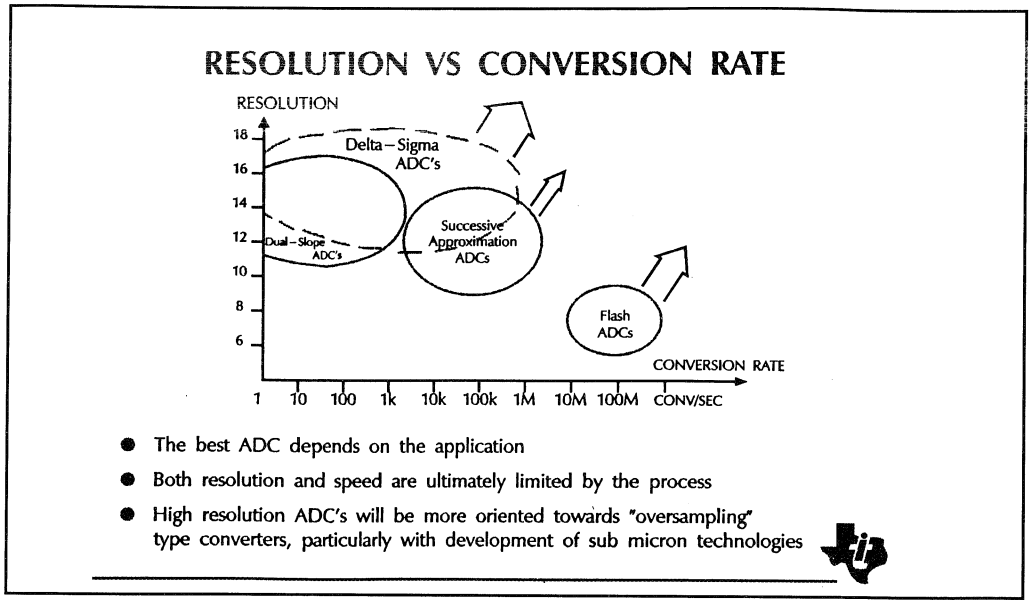
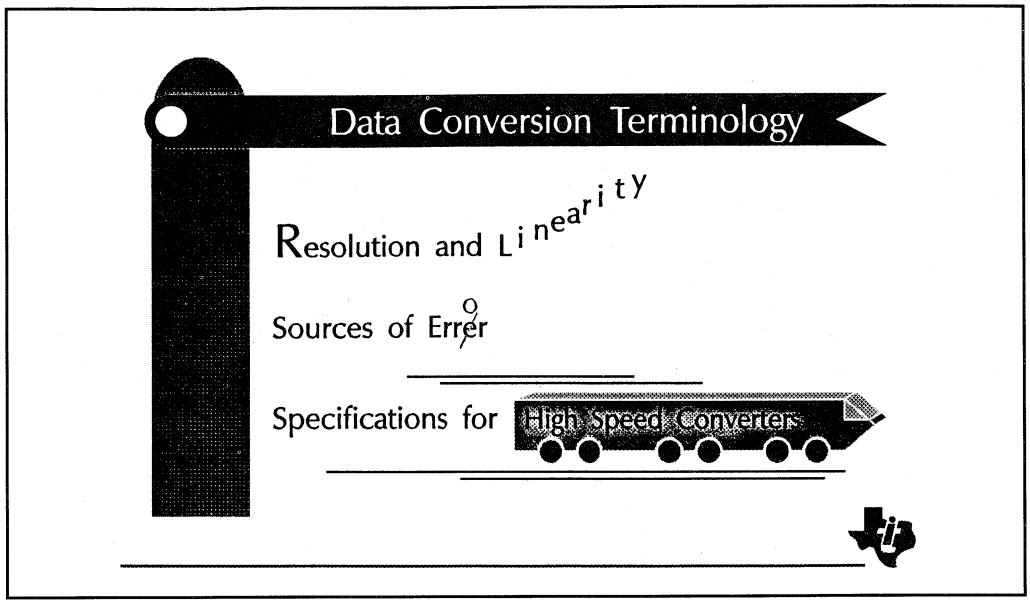


Figure 12 - Resolution and conversion rate

Each type of converter has its own application areas. Today the biggest market is for successive approximation converters used in a variety of applications such as automotive, high performance signal processing and general industrial applications. Dual slope converters are mainly used in metering type of applications or for conversion of slowly changing signals like temperature. Delta-sigma conversion technique is expected to replace many of these application over the next decade. The flash converters market is also growing fast due to the increased demand for video signal processing and other applications in the consumer segment of the market.



Section 2 - Datasheet definitions

This section addresses the way the specifications for a data converter are defined on a manufacturers datasheet. It covers the sources of error that change the characteristics of the device from an ideal function to reality.

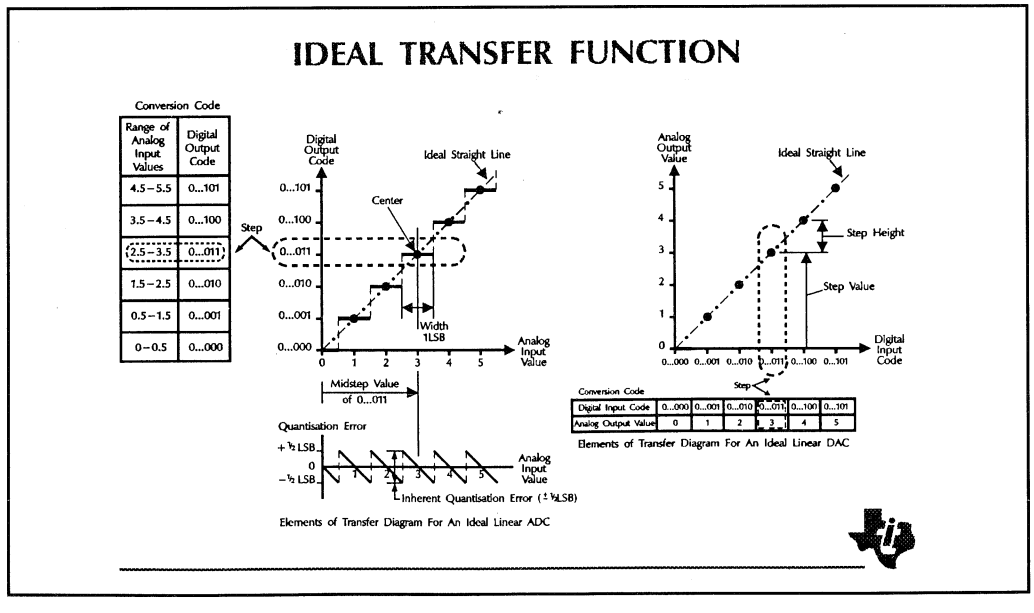


Figure 13 - The Ideal transfer function

13.1 Analogue to Digital Converter (ADC)

An ideal ADC uniquely represents all analogue inputs within a certain range by a limited number of digital output codes. The diagram shows that each digital code represents a fraction of the total analogue input range.Since the analogue scale is continuous, whilst the digital codes are discrete, there is a quantisation process that introduces an error. As the number of discrete codes increases, the corresponding step width gets smaller and the transfer function approaches an ideal straight line. The steps are designed to have transitions such that the midpoint of each step corresponds to the point on this ideal line.

The width of one step is defined as 1 LSB (one **L**east **S**ignificant **Bit**) and this is often used as the reference unit for other quantities in the specification. It is also a measure of the resolution of the converter since it defines how many portions the full analogue range is divided into. Hence, 1/2 LSB represents an analogue quantity equal to a half of the analogue resolution.

The ***Resolution*** of an ADC is usually expressed as the number of bits in its digital output code. For example, an ADC with an n-bit resolution has 2^n possible digital codes which define 2^n step levels. However, since the first (zero) step and the last step have only half the full width, the Full Scale Range (FSR) is divided into $2^n - 1$ step widths. Hence

$$1\ LSB = FSR / (2^n - 1) \quad \text{for an n-bit converter} \qquad 13.1.1$$

13.2 Analogue to Digital Converter (DAC)

A DAC represents a limited number of discrete digital input codes by a corresponding number of discrete analogue output values. Therefore, the transfer function of the DAC is a series of discrete points . For a DAC, 1 LSB corresponds to the height of a step between successive analogue outputs, with the value defined in the same way as for the ADC in 13.1.1. A DAC can be thought of as a digitally controlled potentiometer whose output is a fraction of the full scale analogue voltage determined by the digital input code.

Sources of Static errors

Static errors , that is those errors that affect the accuracy of the converter when it is converting static (D.C.) signals, can be completely described by just four terms.These are ***Offset*** error, ***Gain*** error, ***Integral nonlinearity*** and ***Differential nonlinearity***. Each can be expressed in LSB units or sometimes as a percentage of the FSR. For example, an error of 1/2 LSB for an 8 bit converter corresponds to 0.2% FSR.

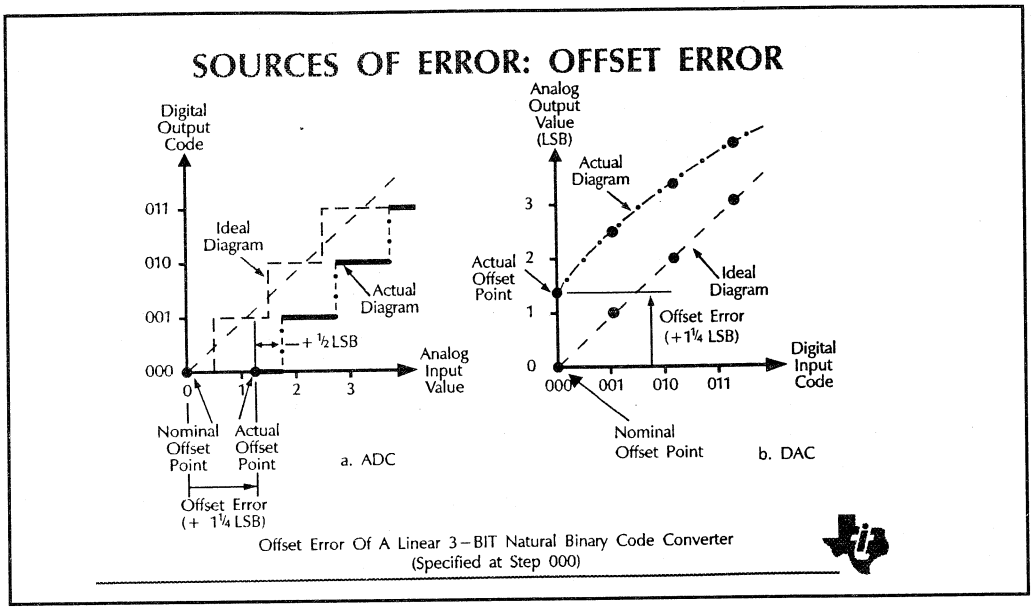


Figure 14 - Offset error

The offset error is defined as the difference between the nominal and actual offset points as shown . For an ADC, the offset point is the midstep value when the digital output is zero, and for a DAC it is the step value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated for by a trimming process. If trimming is not possible, this error is referred to as the zero scale error.

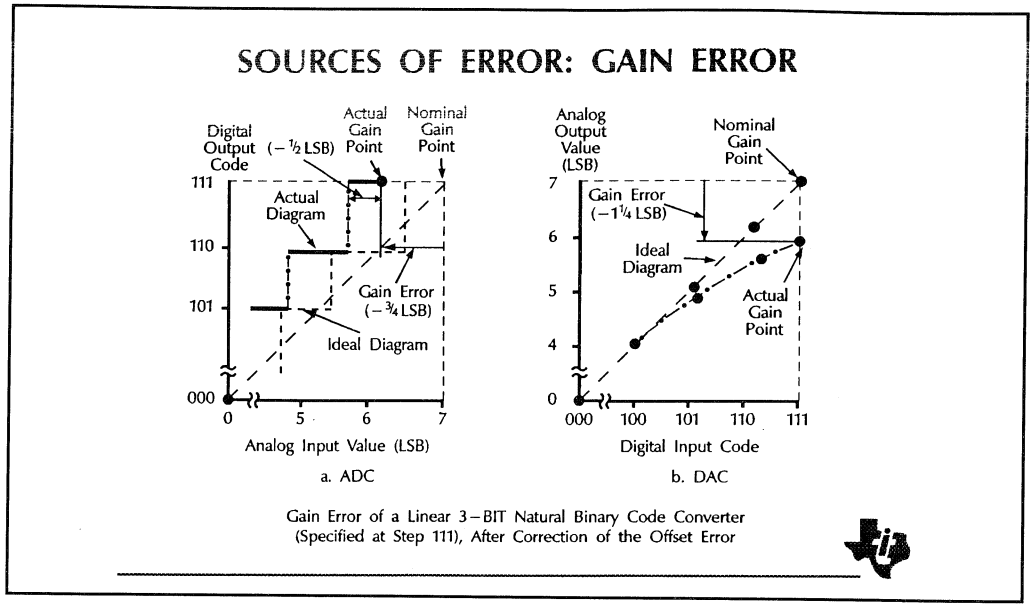


Figure 14.1 - Gain error

The gain error is defined as the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero. For an ADC, the gain point is the midstep value when the digital output is full scale, and for a DAC it is the step value when the digital input is full scale. This error represents a difference in the slope of the actual and ideal transfer functions and as such corresponds to the same percentage error in each step. This error can also usually be adjusted to zero by trimming.

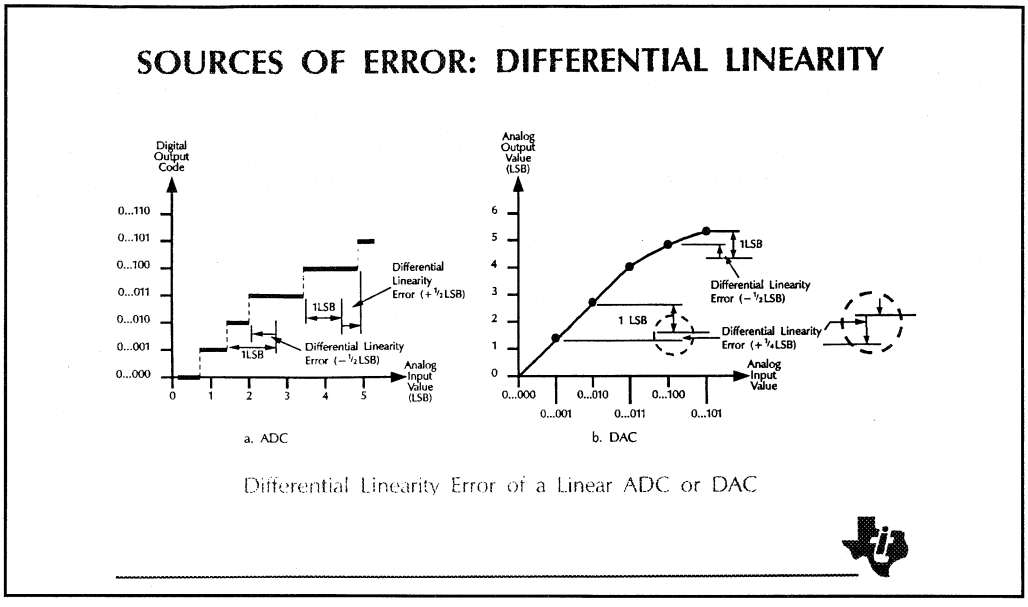


Figure 14.2 - Differential Non-Linearity (DNL)

The differential non-linearity error is the difference between an actual step width (for an ADC) or step height (for a DAC) and the ideal value of 1 LSB. Therefore if the step width or height is exactly 1 LSB, then the differential non-linearity is zero. If the DNL exceeds 1 LSB, there is a possibility that the converter may become non-monotonic. This means that the magnitude of the output gets smaller for an increase in the magnitude of the input. In an ADC there is also a possibility that there will be missing codes i.e. one or more of the possible 2^n binary codes are never output.

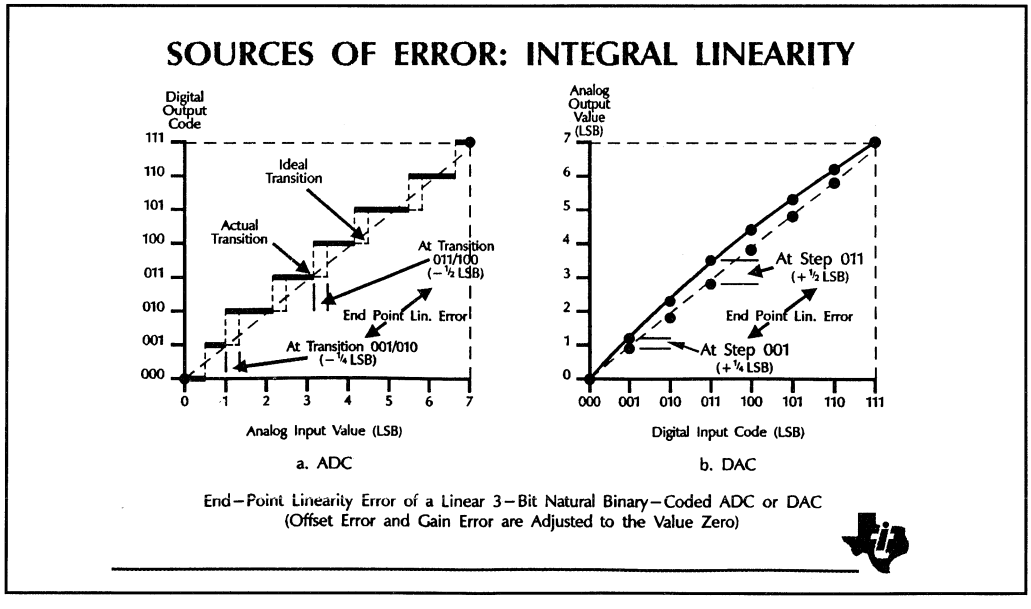


Figure 14.3 - Integral Non-Linearity (INL)

The integral non-linearity error (sometimes seen as simply linearity error) is the deviation of the values on the actual transfer function from a straight line. This straight line can be either a "best straight line" which is drawn so as to minimise these deviations or it can be a line

drawn between the end points of the transfer function once the gain and offset errors have been nullified. The second method is called "end-point" linearity and is the usual definition adopted since it can be verified more directly.

For an ADC the deviations are measured at the transitions from one step to the next, and for the DAC they are measured at each step. The name integral non-linearity derives from the fact that the summation of the differential non-linearities from the bottom up to a particular step, determines the value of the integral non-linearity at that step.

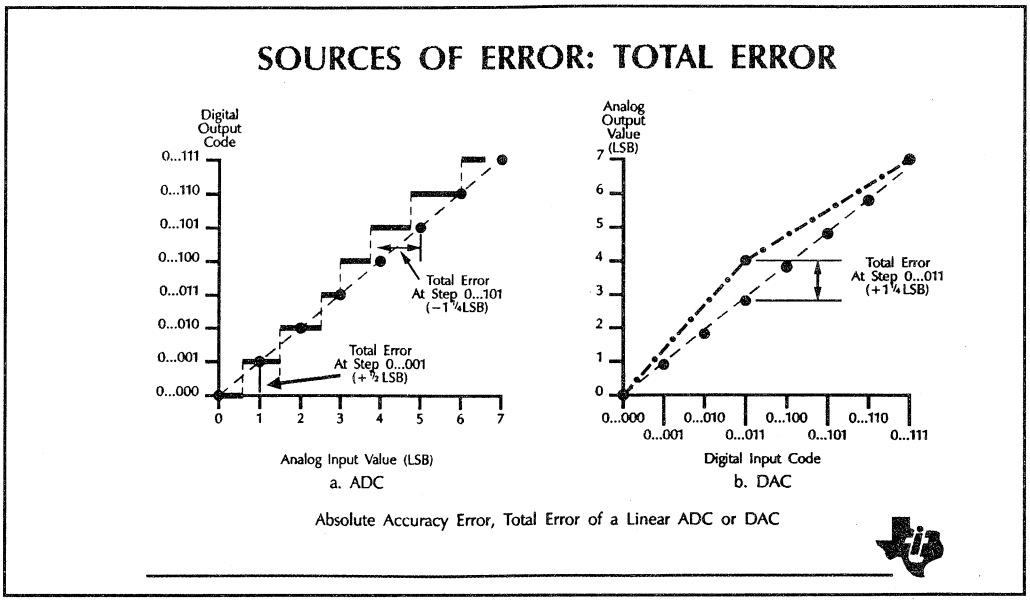


Figure 14.4 - Absolute accuracy error

The absolute accuracy error or total error of an ADC is the maximum value of the difference between an analogue value and the ideal midstep value within any step. For a DAC it is the difference between the step value and the ideal step value. It includes the effects of offset, gain and integral linearity errors and also the quantisation error in the case of an ADC.

Specifications for flash converters

The arrival of flash converters has made it possible to use digital processing in applications that were previously entirely analogue. Digital television is a prime example of this. However, with the introduction of these devices came the introduction of new specifications to define their performance. This section defines some of these.

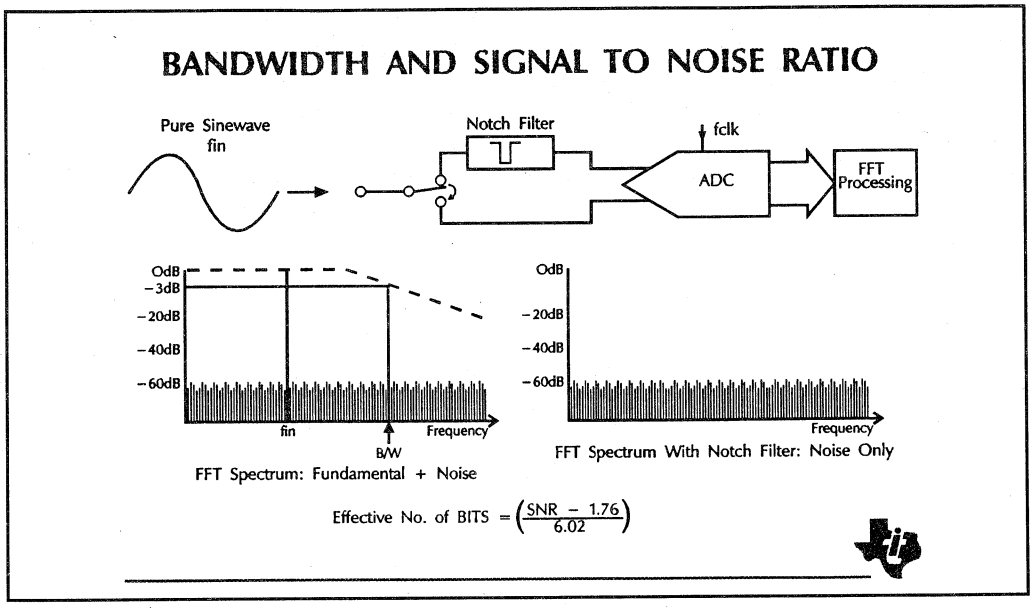


Figure 15 - Bandwidth

The bandwidth of a high speed ADC is defined as the frequency of the analogue input signal whose output amplitude is 3dB down when the converter is operating at its maximum conversion rate. This can be measured either by reconstructing the output using a reference DAC or else by performing an FFT (Fast Fourier Transform) on the output and comparing the spectrum with the fundamental.

Another factor that limits the bandwidth is the possibility of spurious "speckle" or missing codes. These are caused by the different propagation delays through the comparators measuring the input signal. As the slew rate of the input increases there is an increased possibility of errors at the point where the comparators change from high to low. Instead of a bank of comparators all reading "1" up to a point and then the rest reading "0", a so called "bubble" can occur when a "0" is found between two "1"s. When this is decoded, it is a non-recognised code which often is translated to full scale or zero , so producing a spurious code at the output. In some converters, this occurs before the 3dB bandwidth as defined above.

Many flash converters make use of a Gray code in the decoding process to help reduce this effect. The Gray code has the advantage that consecutive codes differ by only one bit change (compared to natural binary where all the bits change at the midscale) so that this error can be minimised.

15.1 - Signal-to-noise ratio and effective bits

For a full-scale sinewave input , the theoretical SNR for an N bit converter is given by

$$SNR = 6.02N + 1.76 \text{ dB} \qquad 15.2.1$$

(This will be derived later on - see number 17 Quantisation)

The normal way of measuring the SNR for a flash converter is to digitise a full scale sinewave and then perform an FFT on the output. The rms power of the fundamental is then compared to the noise floor by inserting a notch filter at the input frequency so that the output is purely due to the effects of noise. The ratio of the two is taken to give a direct measurement of the SNR. This measurement can then be used to determine the number of ***effective bits*** of accuracy the converter displays at that frequency. For example, a nominal 8 bit resolution ADC may be specified as having 45dB SNR at a particular input frequency. The number of effective bits is defined as

$$N_{EFF} = (SNR-1.76)/ 6.02 = 43.24 / 6.02 = 7.2 \text{ bits} \qquad 15.2.2$$

The actual performance of the device is therefore worse than its nominal spec at this frequency.

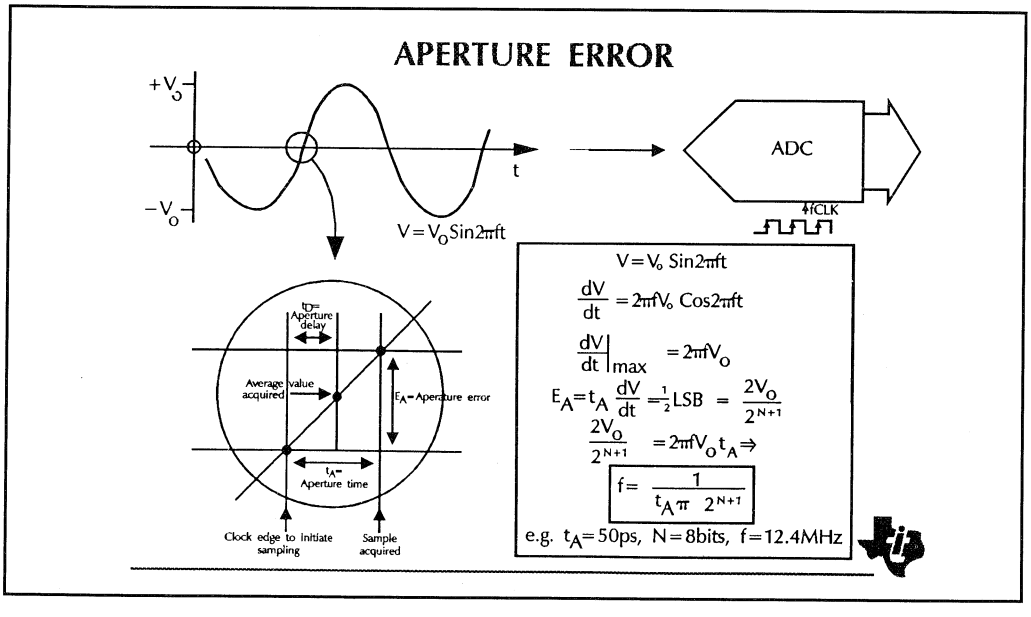


Figure 15.2 - Aperture error

Aperture error is caused by the fact that whilst in theory a sample can be taken instantaneously, in practice it takes a finite length of time. Therefore, during the time the sample clock initiates a sample ,to the time when the sample and hold circuit on the input has acquired it, the input signal has changed. To a first order approximation, if the input varies linearly with a slope dV/dt , then the aperture error can be expressed as

$$E_A = T_A \, dV/dt \qquad 15.3.1$$

where TA is the ***aperture time***. The actual value of the input acquired will be the average value of the input during T_A. The time between the leading edge of the sample clock and the moment at which the input reaches this average value is called the ***aperture delay***. The importance of this parameter is that it allows a designer to determine the relationship needed between the clock and the input signal to sample at a particular point on the input.

For an ideal case, the effect of the aperture error would be zero since the delay and the aperture time would be constant and hence the actual value acquired would always be correct. In practice, however, true errors are caused by variations in the delay due to ***aperture jitter***. This variation is caused by noise on the clock or the input signal which can change the delay .

The effect of the aperture error is to set another limitation on the maximum frequency of the input sinewave because it defines the maximum slewrate of that signal. For a sinewave input as shown, the value of the input V is defined as

$$V=V_0 \text{ Sin } 2\pi ft \qquad 15.3.2$$

The maximum slewrate occurs at the zero crossing point and is given by

$$dV/dt \Big|_{MAX} = 2\pi f V_0 \qquad 15.3.3$$

If the aperture error is not to affect the accuracy of the converter, it must be less than 1/2 LSB at the point of maximum slewrate. For an N bit converter therefore

$$E_A = t_A \, dV/dt = 1/2 \text{ LSB} = 2V_0/2^{N+1} \qquad 15.3.4$$

Substituting 15.3.3 into this gives

$$2V_0 / 2^{N+1} = 2\pi f V_0 t_A \qquad 15.3.5$$

So that the maximum frequency is given by

$$f_{MAX} = 1 / (t_A \, \pi \, 2^{N+1}) \qquad 15.3.6$$

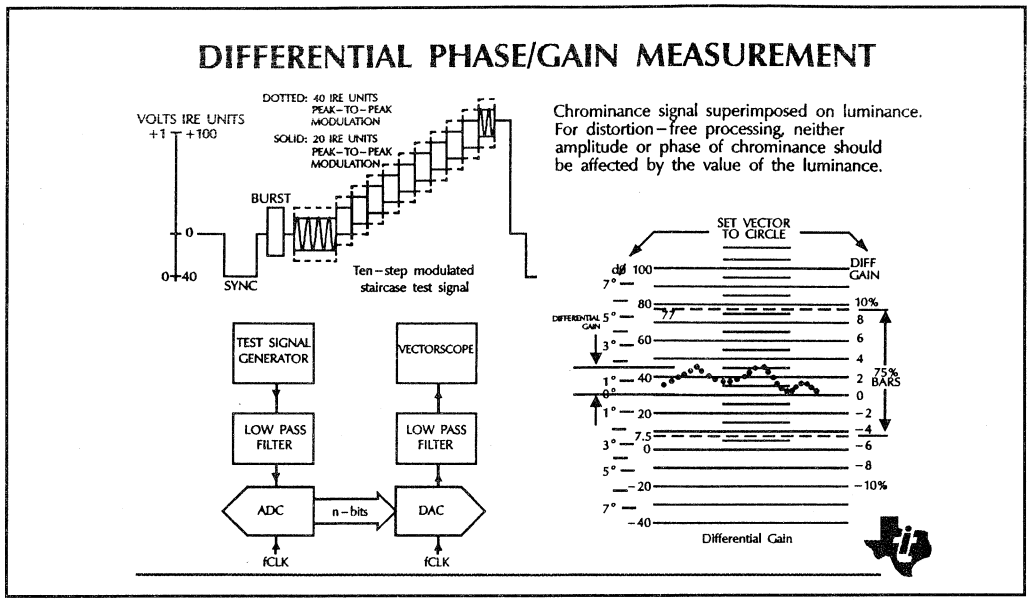
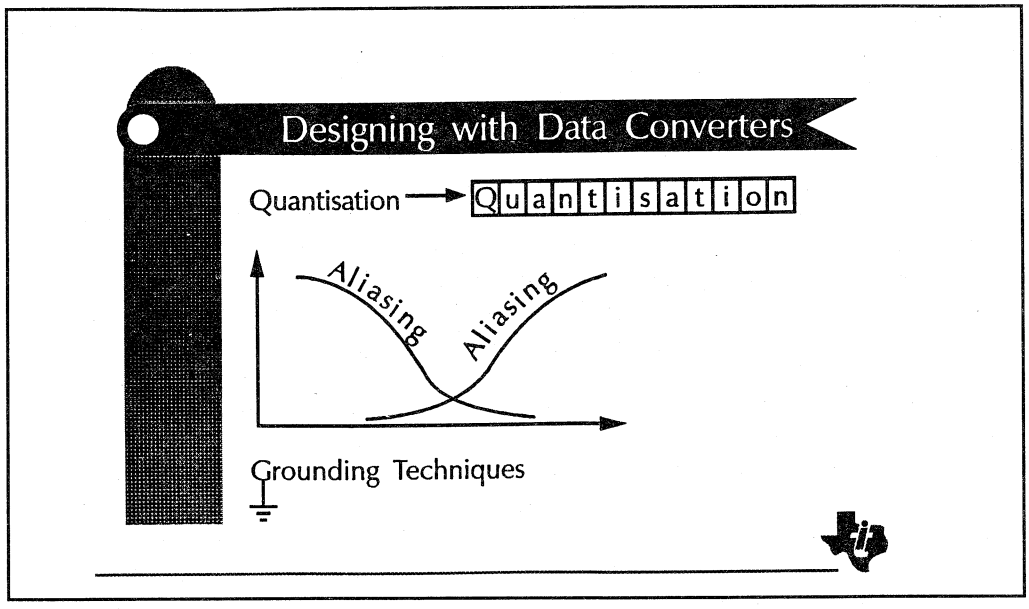


Figure 15.3 - Differential Phase and Gain

Differential gain is defined as "the percentage difference between the output amplitude of a small high frequency sinewave at two stated levels of a low frequency signal on which it is superimposed." Differential phase is similarly defined for the output phase difference in degrees, of the two signals.

These definitions are of direct relevance in video applications. A colour signal is represented by a small amplitude, high frequency Chrominance signal which determines the colour saturation, and a lower frequency Luminance signal which determines the brightness and onto which the chrominance signal is superimposed. For distortion-free processing, it is important that neither the amplitude or phase of the chrominance is affected by the value of the luminance signal.

Measurements of DG and DP are made using the set up shown , using a standard video test signal (NTSC ramp). This can be either a staircase as shown or a continuous ramp. In each case, the device being tested (ADC or DAC) is used in conjunction with a reference device whose DP and DG are already known. The vectorscope makes a direct measurement of the DP and DG but the trace is unclear because of the quantising effects of the DAC. Hence, the measurement is made from the centre of the trace as shown.



Section 3 : Designing with data converters

This section considers some of the aspects of designing with data conversion products . In each case, the background theory is presented along with examples of how it can be applied to real designs. A design example is presented to conclude the section.

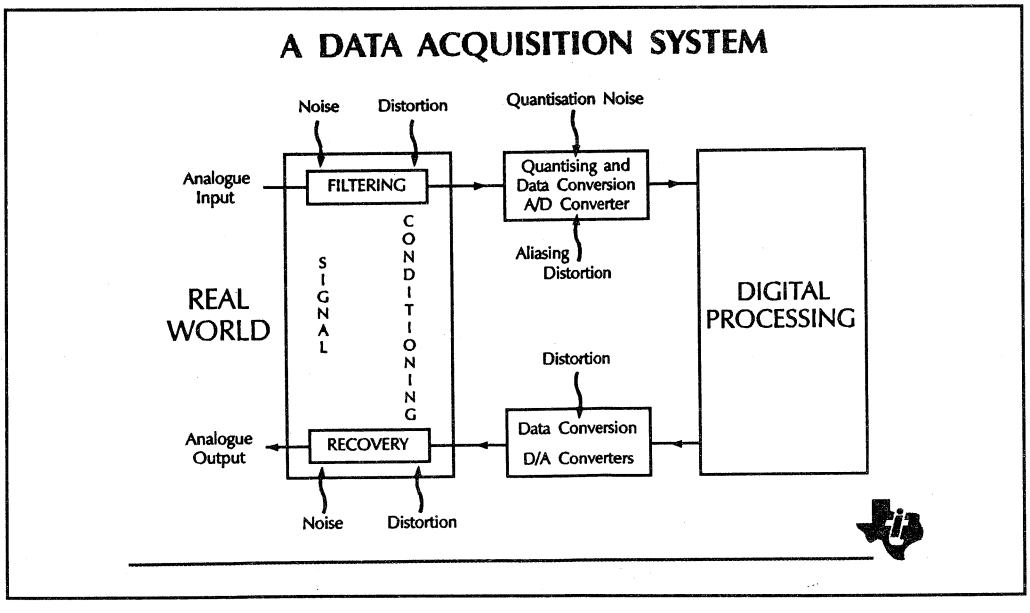


Figure 16 - Data acquisition systems

As for any system, a system to acquire data is made up of some key elements supported by secondary functions. The contribution made by each component to the performance of the system must be examined separately , if the performance of the whole is to meet its design goals.

The diagram shows the two basic elements which subdivide the system and convert the real world signals into the digital data for the processor. These are the Input/Output stage and the conversion stage.

16.1 Input/Output stage

The input/output stage to the system consists of an analogue processing function. This can vary from simple a.c. coupling to remove large d.c. offsets, up to extensive frequency waveshaping to improve the dynamic range of the system.

Normally this analogue processing is done with individual op-amps configured to give the required frequency response. Since any signal must pass through the I/O stage to reach the conversion section, it is important to recognise that any noise or distortion introduced will become part of the signal that is converted. Hence , the choice of components for the I/O stage is crucial to the satisfactory performance of the system as a whole.

The concept of bits of accuracy of an op-amp (as detailed in the signal conditioning section) is a useful one in this context. Using an op-amp that has the same bits of accuracy as the number of bits in the converter will introduce a 3dB loss in the SNR of the system . It is hence important to use low noise op amps with high input impedance for the input stage.

The trend to increased system integration means that this filtering is increasingly being carried out using integrated circuits that employ a switched capacitor technique. The benefits of switched capacitor filters in certain applications are numerous. They are easily programmed to give a certain response and track accurately because of good capacitor matching on chip.

They provide a compact solution to filter design since large capacitors and inductors are not needed and small values in the range 5 to 20 pF are sufficient.

In summary, the design of the I/O stage is vital to the overall system. The techniques required have already been addressed in the signal conditioning section, and so apart from switched capacitor filters, will not be considered further here.

16.2 Conversion stage

The next part of the system is the true data-acquisition area which includes the ADC and the DAC. The choice is made here in terms of both resolution and accuracy and the method of conversion required as outlined earlier.

The nature of the quantisation process introduces distortion of the input signal, and the effect of sampling produces the phenomenon called Aliasing . Quantisation and aliasing are the first things we will consider now.

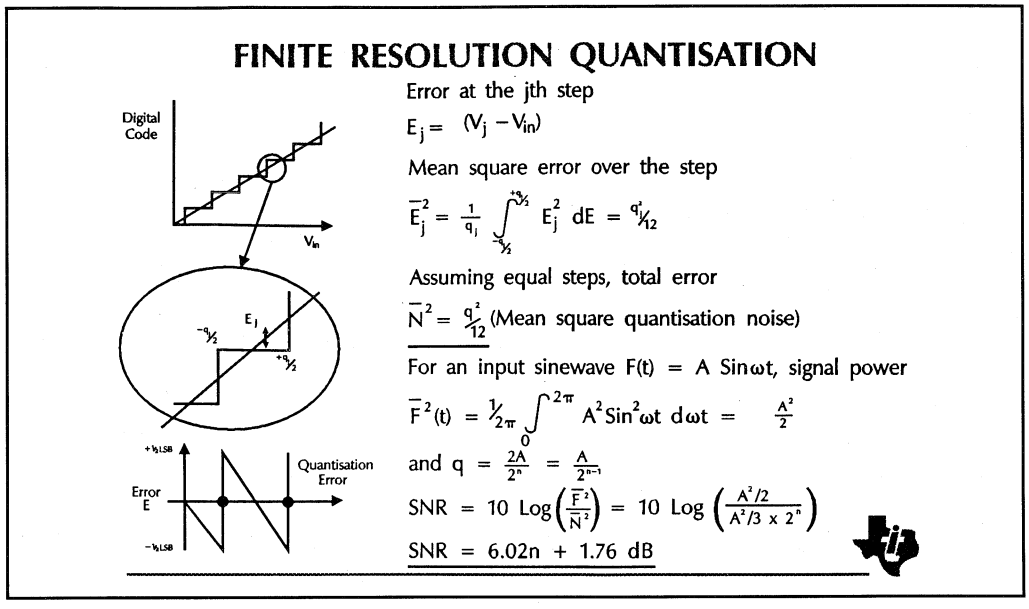


Figure 17 - Quantisation effects

It is clearly apparant that the real world analogue input to an ADC is a continous signal with an infinite number of possible states, whereas the digital output is by its nature a discrete function with a number of different states determined by the resolution of the device. It follows from this therefore, that in converting from one form to the other, certain parts of the analogue signal that were represented by a different voltage on the input , are represented by the same digital code at the output. Some information has been lost and distortion has been introduced into the signal. This is ***Quantisation noise***.

If we take an ideal staircase transfer function of the ADC, the error between the actual input and its digital form will have a uniform probability density function if the input signal is assumed to be random. It can vary in the range +/- 1/2 LSB or +/- q/2 where q is the width of a step.

$$p(\epsilon) = 1/q \quad (-q/_2 <= \epsilon <= +q/_2) \qquad 17.1.1$$
$$p(\epsilon) = 0 \quad \text{(otherwise)}$$

The average noise power (mean square) of the error over a step is given by

$$E^2(\epsilon) = \int_{-q/_2}^{+q/_2} p(\epsilon)^2 \, d\epsilon \qquad 17.1.2$$

which gives $E^2(\epsilon) = q^2/12$ 17.1.3

The total mean square error, N^2, over the whole conversion area will be the sum of each quantisation levels mean square multiplied by its associated probability. Assuming the converter is ideal, the width of each code step is identical and therefore has an equal probability. Hence for the ideal case

$$N^2 = q^2/12 \qquad 17.1.4$$

Considering a sinewave input F(t) of amplitude A so that

$$F(t) = A\sin \omega t \qquad 17.1.5$$

which has a mean square value of $F^2(t)$, where

$$F^2(t) = 1/2\pi \int_0^{2\pi} A^2 \sin^2 \omega t \, d\omega t = A^2/2 \qquad 17.1.6$$

which is the signal power. Therefore the signal to noise ratio SNR is given by

$$SNR\ (dB) = 10\ Log\ [(A^2/2)/(q^2/12)] \qquad 17.1.7$$

$$But\ q = 1LSB = 2A/2^n = A/2^{n-1} \qquad 17.1.8$$

Substituting for q in 17.1.7 gives

$$SNR = 10\ Log\ [(A^2/2)/(A^2/3x2^n)] = 10\ Log\ (3x2^{n-1})$$
$$= \underline{6.02n + 1.76\ dB} \qquad 17.1.9$$

This gives the ideal value for an n bit converter . This shows that each extra 1 bit of resolution provides approximately 6dB improvement in the SNR.

In practice, the errors mentioned in section 2 will introduce non-linearities that lead to a reduction of this value. The limit of a 1/2 LSB linearity error is a missing code condition which is equivalent to a reduction of 1 bit of resolution and hence a reduction of 6dB in the SNR. This then gives a worst case value of SNR for an n-bit converter with 1/2 LSB linearity error.

$$SNR\ (worst\ case) = 6.02n + 1.76 - 6 = \underline{6.02n - 4.24\ dB} \qquad 17.1.10$$

Hence we have established the boundary conditions for the choice of the resolution of the converter based upon a desired level of SNR.

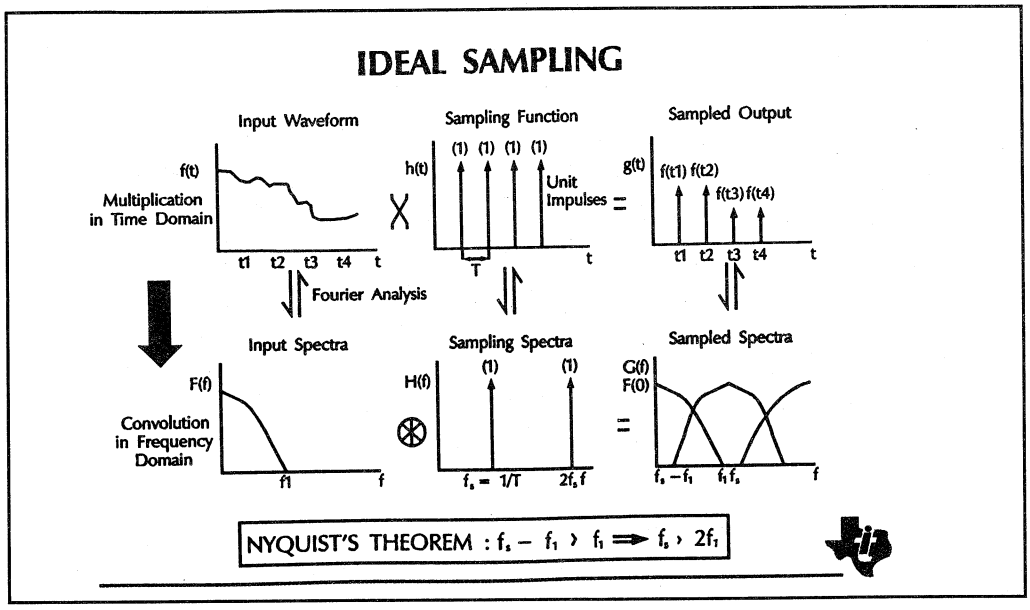


Figure 18 - Ideal sampling

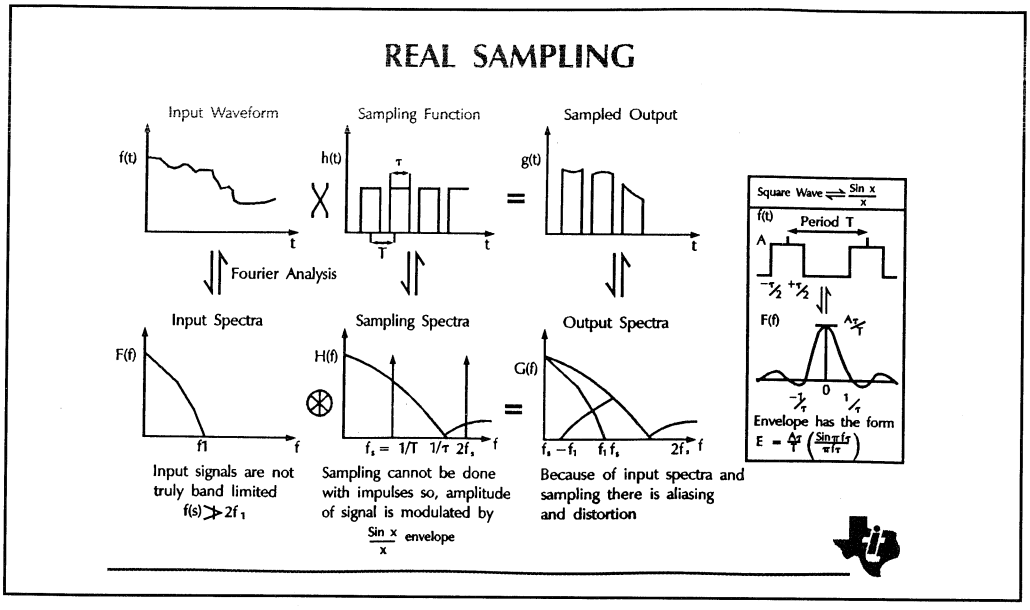
In converting a continuous time signal into a discrete digital representation, the process of sampling is a fundamental requirement. In an ideal case, sampling takes the form of a pulse train of impulses which are infinitessimally narrow yet have unit area. The time between each impulse is called the sampling rate. The input signal too is idealised by being truly bandlimited, containing no components in its spectrum above a certain value.

The ideal sampling condition is shown here, represented in both the frequency and time domains. The effect of sampling in the time domain is to produce an amplitude modulated train of impulses representing the value of the input signal at the instant of sampling. In the frequency domain, the spectrum of the pulse train is a series of discrete frequencies at multiples of the sampling rate. Sampling convolves the spectra of the input signal with that of the pulse train to produce the combined spectrum shown , with double sidebands around each discrete frequency which are produced by the amplitude modulation. In effect some of the higher frequencies are "folded back" so that they produce interference at lower ones. This interference causes distortion which is called ***Aliasing***.

If we assume the input signal is bandlimited to a frequency f_1 , and is sampled at frequency f_s, it is clear from the diagram that the overlap (and hence aliasing) will not occur if

$$f_1 < f_s - f_1 \qquad \text{so that} \quad 2f_1 < f_s \qquad 18.1.1$$

Therefore if sampling is done at a frequency at least twice as great as the maximum frequency of input signal, no aliasing will occur and all the signal information can be extracted. This is ***Nyquist's theorem***, and it provides the basic criteria for the selection of the sampling rate required by the converter to process an input signal of a given bandwidth.



Foil 19 - Real sampling

The concept of an impulse is a useful one to simplify the analysis of sampling. However, it is a theoretical ideal which can be approached but never reached in practice. Instead the real signal will be a series of square waves of period equalling the reciprocal of the sampling frequency. The sample is acquired over a period t which is normally much smaller than the period T. The result of sampling with this pulse train is a series of amplitude modulated pulses.

Examining the spectrum of the square wave pulse train shows a series of discrete frequencies as with the impulse train, but the amplitude of these frequencies is modified by an envelope which is defined by $\mathrm{Sin}x/x$ (sometimes written $\mathrm{Sinc}(x)$) where x in this case is πf_s . For a square wave of amplitude A, the envelope of the spectrum is defined as

$$\text{Envelope} = A\,\tau / T\ [\ \mathrm{Sin}\ (\pi f_s\ \tau)]\ /\pi f_s\ \tau \qquad 19.1.1$$

This effect further aggravates the problem of aliasing. It is minimised by ensuring that the sampling time is small in comparison with the sampling rate T.

It is also much more pronounced for DACs due to the fact that with a DAC the power output of the codes widths are transferred to the output of the system. For maximum power in the signal out ,zero order hold DACs are used so that the pulse width normally lasts the whole sampled period. The error resulting from this can be controlled with a filter which compensates for the Sinc envelope. This can be implemented as a digital filter, in a DSP , or using conventional analogue techniques. The TLC32044 Analogue interface circuit featured in section 4 has an on-chip Sinc correction filter after its DAC output for this purpose.

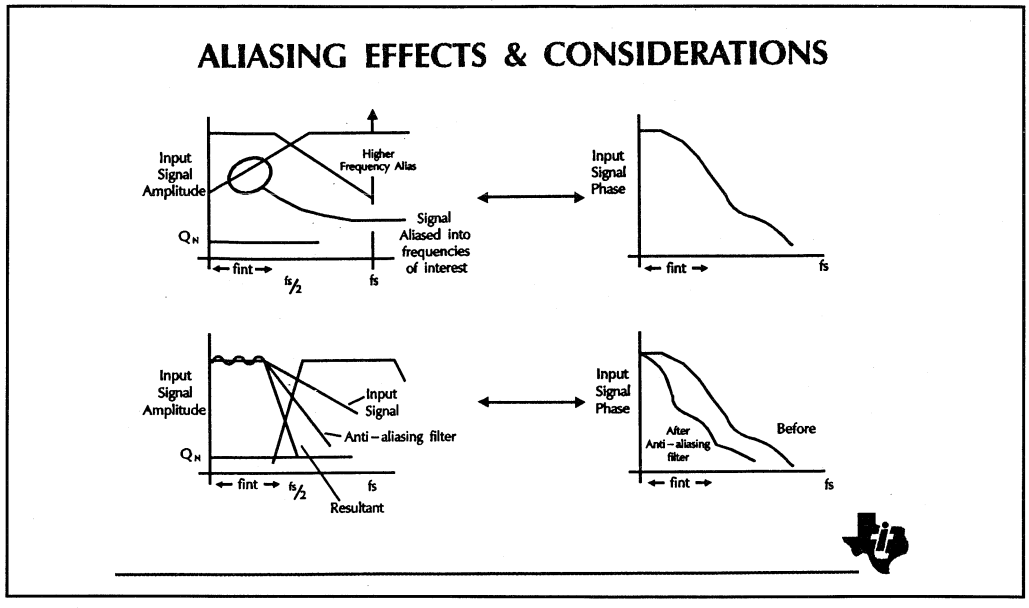


Figure 20 - AC effects and aliasing considerations

No signal is truly deterministic and therefore in practice has infinite bandwidth.However, the energy of higher frequency components gets increasingly smaller so that at a certain value it can be considered to be irrelevant. This value is a choice that must be made by the system designer.

As we have seen, the amount of aliasing will be affected by the sampling frequency and by the relevant bandwidth of the input signal, filtered as required. The factor that determines how much aliasing can be tolerated is ultimately the resolution of the system. If the system has low resolution then the noise floor is already relatively high and aliasing may not have a significant effect. However, with a high resolution system , aliasing may increase the noise floor considerably and therefore needs to be controlled more completely.

The sampling rate is the easiest way to prevent aliasing as we have seen. However, there will be a limit on what frequency this can be, determined by the type of converter used and also possibly by the maximum clock rate of the digital processor receiving and transmitting the data. Therefore, to reduce the effects of aliasing to within acceptable levels, analogue filters must be used to alter the input signal's spectrum.

20.1 Choice of filter

Just as we have already seen with sampling , there is an ideal solution to the choice of filter and a practical realisation that has to make compromises. The ideal filter is a so-called ***brickwall*** filter which introduces no attenuation in the passband, and then cuts down instantly to infinite attention in the stopband. In practice , this is approximated by a filter that introduces some attenuation in the passband, has a finite rolloff , and passes some frequencies in the stopband. It may also introduce phase distortion as well as amplitude distortion. The choice of the filter order and type must be decided upon so as to best meet the requirements of the system.

20.2 Types of filter

The basic types of filter available to the designer are briefly presented here for comparison. This is not intended to be a full analysis of the subject and the reader should refer to other texts for more details.

20.2.1 Butterworth filter

A Butterworth or maximally flat filter is the most commonly used general purpose filter. It has a monotonic passband with the attenuation increasing up to its 3-dB point which is known as the natural frequency. This frequency will be the same whatever the order of the filter is . However, by increasing the order of the filter, the roll-off in the passband moves closer to its natural frequency and the roll-off in the transition region between the natural frequency and the stopband becomes sharper.

20.2.2 Chebyshev filter

The Chebyshev equal ripple filter distributes the roll-off accross the whole passband . Hence, it introduces more ripple in the passband but provides a sharper roll-off in the transition region. This type of filter has poorer transient and stepping responses due to its higher Q values in stages of the filter.

20.2.3 Inverse Chebyshev filter

Both the Butterworth and Chebyshev filters are monotonic in the transition region and stopband. By allowing ripple in the stopband it is possible to make the roll-off sharper still. This is the principle of the Inverse Chebyshev, based on the reciprocal of the angular frequency in the Chebyshev filter response. This filter is monotonic in the passband, and can be flatter than the Butterworth filter whilst providing a greater initial roll-off than the Chebyshev filter.

20.2.4 Cauer Filter

The Cauer or Elliptical filter is non-monotonic in both the pass and stop bands, but provides the greatest roll-off in any of the standard filter configurations.

20.2.5 Bessel-Thomson Filter

All the types mentioned above introduce non-linearities into the phase relationship of the component frequencies of the input spectrum. This can be a problem in some applications when the signal is reconstructed. The Bessel-Thomson or linear delay filter is designed to introduce no phase distortion but this is acheived at the expense of a poorer amplitude response.

In general, the performance of all of these types can be improved by increasing the number of stages i.e. the order of the filter. The penalty for this of course is the increased cost of components and board space required. For this reason, it may be appropriate to use an integrated solution using switched capacitor filter building blocks which provide comparable performance with a discrete solution over a range of frequencies from about 1kHz to 100kHz . They also provide the designer with a compact cost effective solution .

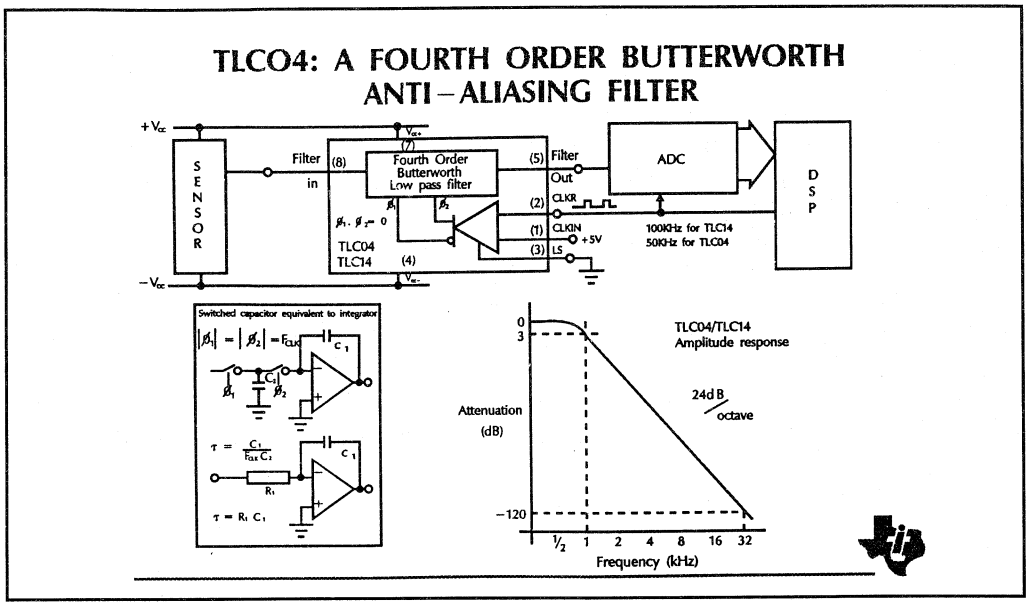


Figure 21 - TLC04 Anti-aliasing Butterworth filter

As detailed previously the Butterworth filter generally provides the best compromise in filter configurations and is by far the easiest to design. The Butterworth filter's characteristic is based on a circle which means that when designing filters, all stages to the filter will have the same natural frequency enabling simpler filter design. Most modern designs which use op-amps are based on building the whole transfer function by a series of second order numerator and denominator stages; a Biquad stage. The Butterworth design is simplified when using these because each stage has the same natural frequency. This can easily be converted to a switched capacitor filter (SCF) which has very good capacitor matching and accurately synthesized RC time constants.

The Switched capacitor technique is demonstrated in the diagram. Two clocks operating at the same frequency but in complete antiphase, alternately connect the capacitor C_2 to the input and the inverting input of an op-amp. During Φ1, charge Q flows onto the capacitor equal to $V_{in}C_2$. The switch is considered to be ideal so that there is no series resistance and the capacitor charges instantaneously. During Φ2, the switches change so that C_2 is now connected to the virtual earth at the op-amp input. It discharges instantaneously delivering the stored charge Q.

The average current that flows I_{av} depends on the frequency of the clocks T so that

$$I_{av} = Q/T = V_{in} C_2/T = V_{in} C_2 F_{clk} \qquad 21.1.1$$

Therefore, the switched capacitor looks like a resistor of value

$$R_{eq} = V_{in} /I_{av} = 1/C_2 F_{clk} \qquad 21.1.2$$

TLC04 Fourth order Butterworth filter

O Low Clock to Cutoff frequency error ... 0.8%
O Cutoff depends only on stability of external clock
O Cutoff range 0.1Hz to 30kHz
O 5V to 12V operation
O Self clocking or both TTL and CMOS compatible

The advantage of the technique is that the time constant of the integrator can be programmed by altering this equivalent resistance, and this is done by simply altering the clock frequency. This provides precision in the filter design, because the time constant then depends on the ratio of two capacitors which can be fabricated in silicon to track each other very closely with voltage and temperature. Note that the analysis assumes V_{in} to be constant so that for an a.c. signal , the clock frequency must be much higher than the frequency of the input .

The TLC04 is one such filter which is internally configured to provide the Butterworth lowpass filter response, whose cut-off frequency is controlled by a digital clock. For this device, the cut-off frequency is set simply by the clock frequency so that the clock to cut-off frequency ratio is 50:1 with an accuracy of 0.8%.This enables the cut-off frequency of the filter to be tied to the sampling rate, so that only one fundamental clock signal is required for the system as a whole. Another advantage of SCF techniques means that fourth order filters can be attained using only one integrated circuit and they are much more easily controlled.

The response of an nth order Butterworth filter is described by the following equation.

$$\text{Attenuation} = [1+ (f/fc)2^n]^{1/2} \qquad 21.1.3$$

For the fourth order realisation in the TLC04, this corresponds to the table below.

Freq	Attenuation		Phase
Fc/2	0.998	0.02dB	26.6
Fc	0.707	3dB	45.0
2Fc	0.0624	24dB	63.4
4Fc	0.00391	48dB	76.0
8Fc	0.000244	72dB	82.9
12Fc	0.000048	86dB	85.2
16Fc	0.000015	96dB	86.4

This means that sampling at 8 times the centre frequency gives an input to aliased signal ratio of 67dB, which is less than ten bit quantisation noise distortion.

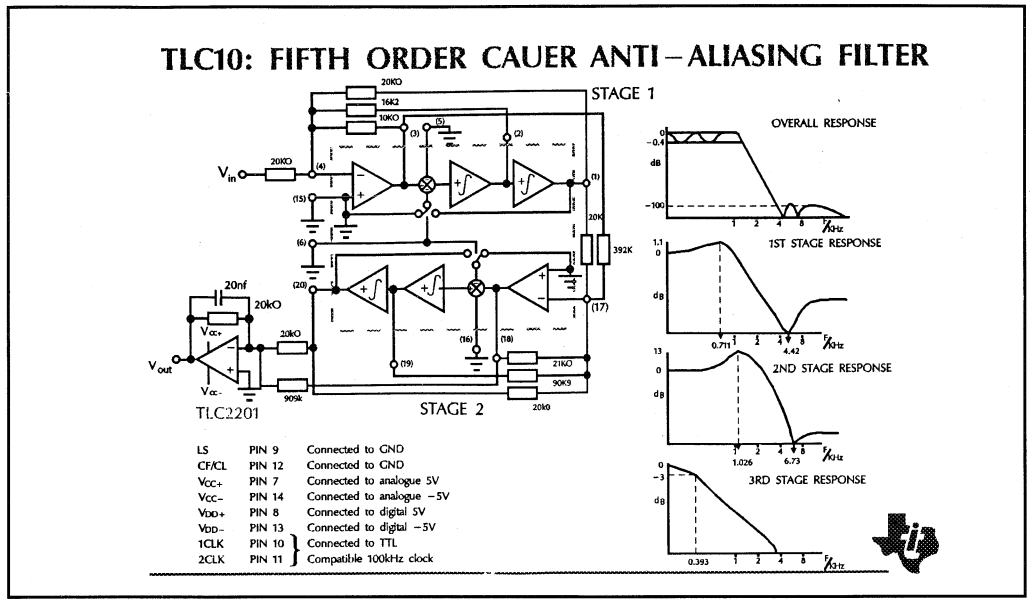


Figure 22 - The TLC10 as an antialiasing Cauer filter.

If a smaller roll-off in the passband and a faster roll-off in the transition region is required so that the signals aliased back into the passband are more attenuated, the Cauer filter can be used to provide this with a smaller order filter.
Switched capacitor filters can be used for this too. The TLC10 is a general purpose SCF building block that contains two independent active filter sections, each of which is designed to provide the response of a second order filter. These can be configured to produce any of the filter types listed in foil 20. In this example , it is configured to realise the Cauer filter configuration.

The Cauer filter has non-monotonic response in both the passband and the stopband. In this application , it is built up from two notch filters and a final low pass filter. The two halves of the TLC10 are used to build the notch filters which are realised as a combination of a low pass filter and a high pass filter . For the first stage, these two components are summed at the input of the second stage. Likewise, for the second stage, the high and lowpass functions are summed using an external summing amplifier built around the TLC2201. This also provides the benefit of further filtering so that the combination becomes a fifth order filter.

TLC10 Universal Dual Switched-capacitor filter

O Low Clock to Cutoff frequency error ... 0.6%
O Cutoff depends only on stability of external clock
O Cutoff range 0.1Hz to 30kHz
O +/-4V to +/-6V operation

As in most filters the lowest Q factor stage is placed first so as to minimise overshoot caused by high frequency elements in the input signal. To enable the op-amps to function properly and without excess distortion, the smallest resistor value is set to be 10k to minimise the current loading .

The fifth order Cauer filter shown is designed to have the following characteristics:

Passband ripple:	0.5 dB
Cut-off frequency:	1 kHz
Stopband frequency:	4 kHz
Stopband attenuation:	97.5 dB

The zeroes and poles are set in the following positions:

1st stage:	f1 = 0.7112 kHz	Q1 = 1.1403 Z1 = 4.4199 kHz
2nd stage:	f2 = 1.0260 kHz	Q2 = 4.4386 Z2 = 6.7342 kHz
3rd stage:	f3 = 0.3933 kHz	

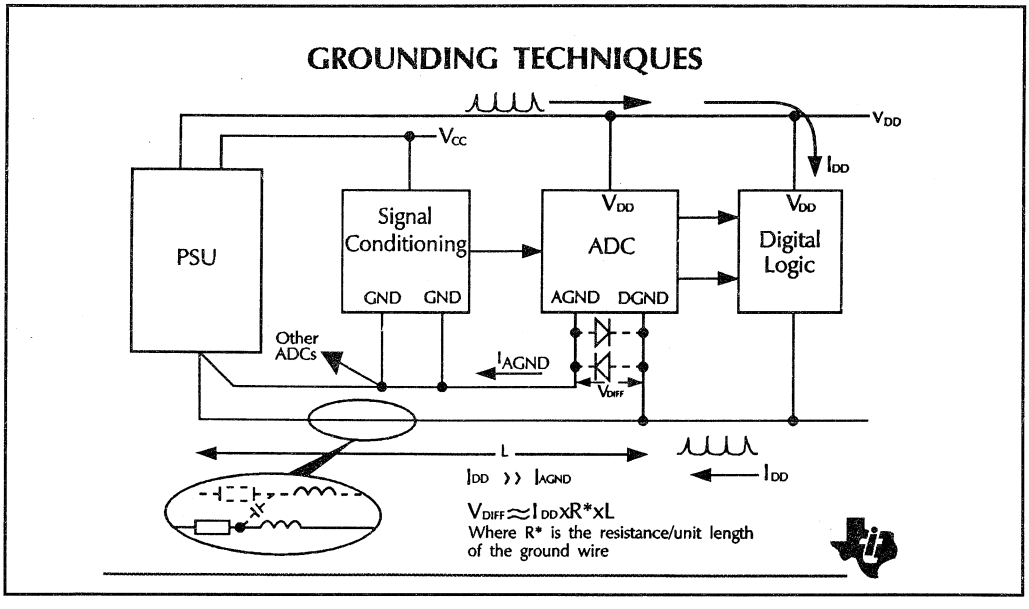


Figure 23 - Grounding techniques

One more area that needs careful consideration is the system of grounding used. It must be remembered that every wire or track on a PCB has a small but finite series resistance and inductance plus some equivalent shunt capacitance.

In a mixed analogue and digital system, it is likely that the digital processor and associated logic will draw the majority of the current . If the return paths for the digital and analogue portions are linked into the same ground rail, the large dc current may cause significant "IR" voltage drops so that the voltage at the various ground points is different. In a high resolution converter such as the 10 bit TLC1540, 1/2 LSB at 5V reference corresponds to only 2.5mV, which can easily be exceeded.

Linking the digital and analogue grounds together also introduces the possibility of current spikes from the high speed switching feeding through to the analogue ground.It is therefore recommended as a minimum that the analogue and digital grounds should be kept separate and should be terminated at the ground of the Power supply unit (PSU). Even better is to provide separate return paths for all currents , tied together only at a single analogue ground reference point.

However, this causes a potential hazard in that the level of the analogue and digital grounds at the ADC may be different. This creates the potential situation whereby the internal diodes may become forward biased and hence cause damage to the device. To prevent this, the analogue and digital grounds at the ADC should be tied together using "nose on tail" diodes. This creates a maximum differential of 1 Vbe drop between the rails, or 0.4V if Shottky diodes are used.

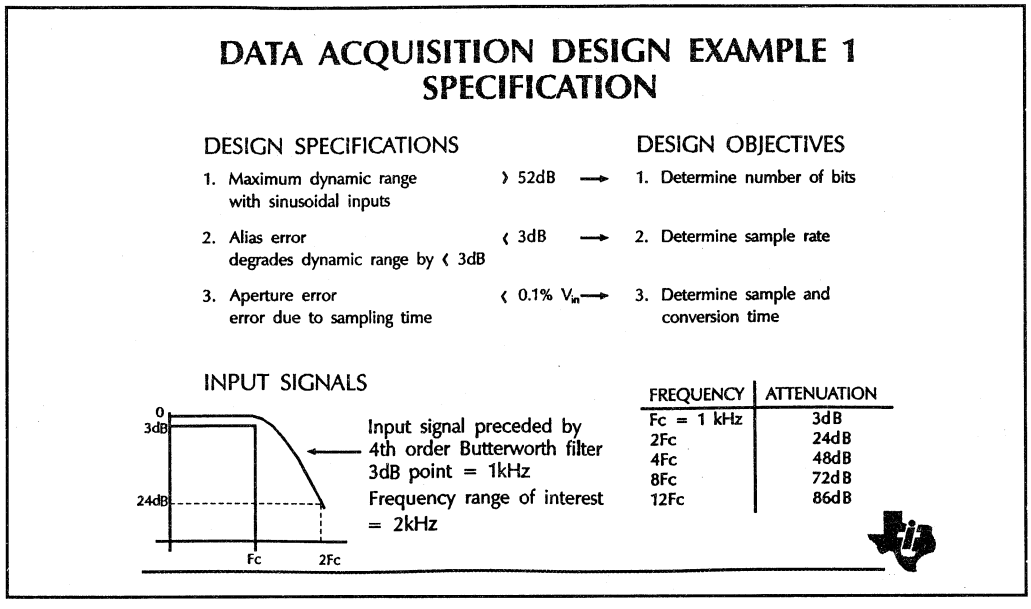


Figure 24 - Design Example 1 : Specification

We have now established some of the parameters that need to be considered when designing a data conversion system. There now follows an example to show how these are brought together in the choice of a suitable conversion device for a particular application. The exact requirements will obviously vary but in general terms these requirements will be Signal to noise ratio (Dynamic range),maximum aliasing error allowed, linearity error and aperture error.

The spectrum of the input signal should also be defined and if necessary it may require an anti-aliasing filter to limit the input bandwidth. In this example it has been assumed that a fourth order Butterworth anti-aliasing filter has been placed before the ADC. This has therefore defined the spectrum of the input signal.

The objective of this example is use an example specification to determine a suitable ADC for the system.

24.1 Example Specification

1. Dynamic range > 52dB (within the frequency of interest)	This will determine the resolution of the ADC
2. Alias error < +3dB above quantisation noise	This will determine the sampling rate
3. Aperture error < 0.1% of max rms input signal	This will determine the conversion time or the sampling rate

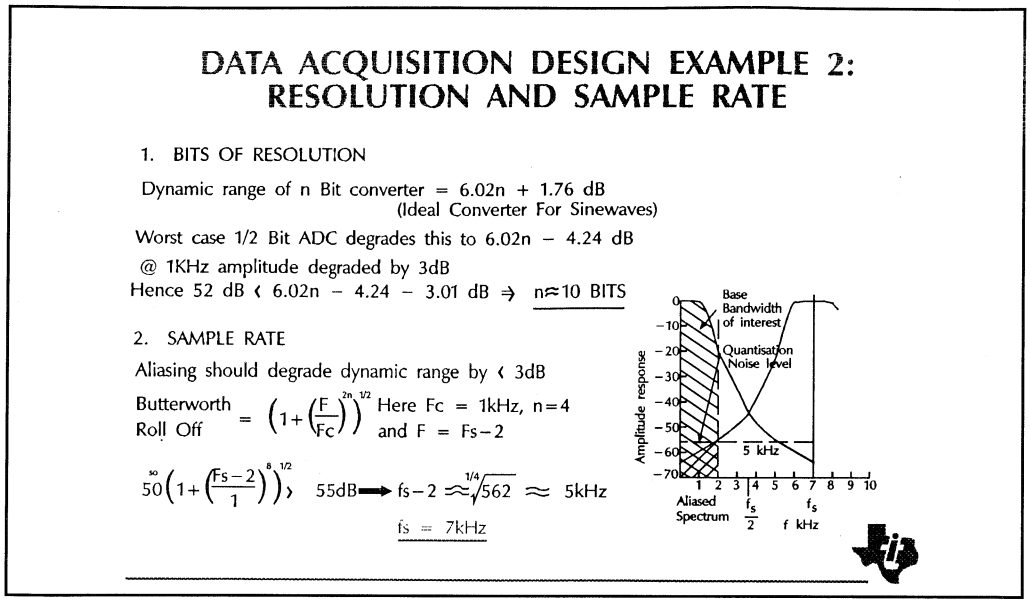


Figure 25 - Design example 2 : Resolution and Speed

25.1 How many bits?

The first decision to be made is on the resolution of the ADC to be used. The dynamic range of the ADC is the basis for this, but assumptions need to be made on the input signal applied. Assuming a sinuisoidal input signal equal to the maximum reference range, the signal to quantisation noise ratio is 6.02n + 1.76 dB for a perfect ADC. However we saw in equation 17.1.10 that this can be reduced to 6.02n - 4.24 dB allowing for non-linearity of 1/2LSB. At 1 kHz , the low pass filter has introduced an attenuation of 3dB so that for a dynamic range of 52 dB the signal quantisation ratio should be better than 55 dB for up to 1 kHz. Therefore taking a worst case for the ADC , the number of bits is given by

$$n = (55 + 4.24)/6.02 = \underline{9.8 \text{ bits}} \qquad 25.1.1$$

so a 10-bit ADC with 1/2 bit linearity error will meet the dynamic range specification.

25.2 How fast?

The spectral content of the input signal has been determined by the Butterworth filter and the requirement of the
specification is for the aliased signal fedback to be less than 3 dB above the quantisation noise level. Assuming that the quantisation noise is flatly spread over the whole sampling frequency and is uncorrelated, the total noise due to aliasing and quantisation is the sum of each individual power associated with them. Hence, the power of the aliased noise should be equal or less than that of the signal to introduce no more than 3dB error. At 1kHz, the signal power is down 3dB from its DC level, so that the aliased power fed back should therefore be less than 55dB.

From equation 21.1.3 Attenuation $A = [1+ (f/f_c)^{2n}]^{1/2}$ 25.2.1

for the Butterworth filter. In this example, the cut off frequency fc = 1kHz and the order of the filter is 4. Substituting in 25.2.1 gives f= 5kHz for A = 55dB. Assuming the maximum signal frequency of interest is 2 kHz, this value occurs at fs - 5kHz which is to be equal to 2kHz. So the minimum sampling frequency is given by

$$fs - 5kHz = 2kHz \Rightarrow \underline{fs = 7kHz} \qquad 25.2.2$$

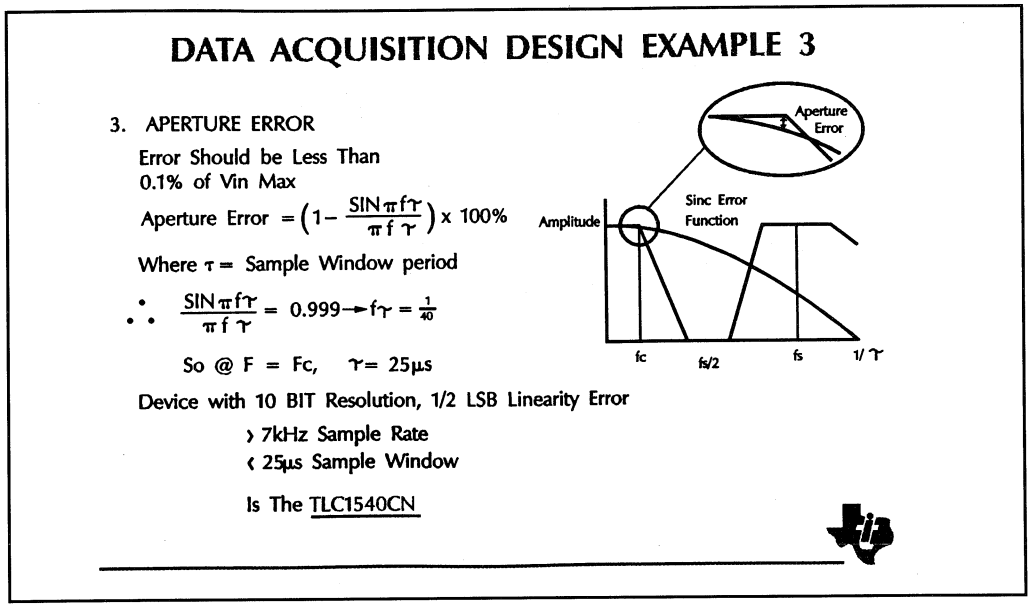


Figure 26 - Design example 3 : Aperture time

The third system specification is the aperture time error, which is related to the length of the sampling period and hence to the conversion time of the ADC.

We have already seen how real sampling with square pulses modulates the spectrum of the input signal with a Sinc($\pi \tau f$) envelope, and that this effect gets worse as the value of τ /T increases.

The error introduced by this factor is given by

$$\text{Aperture error} = [1 - \sin(\pi f \tau) / (\pi f \tau)] \times 100\% \qquad 26.1.1$$

which in this example is required to be less than 0.1%. This can be approximated using a series for Sin x to give

$$\underline{f t = 1/40} \qquad 26.1.2$$

which means that for this error at 1 kHz , a sampling window of 25 µS is needed.

In summary, we require an ADC with the following specification.

1. Resolution 10 bits (at 1/2 LSB linearity)
2. Conversion rate 7kHz
3. Aperture (sample) time 25µS

An ADC that meets this specification is the TLC1540 , a 10 bit successive approximation converter.

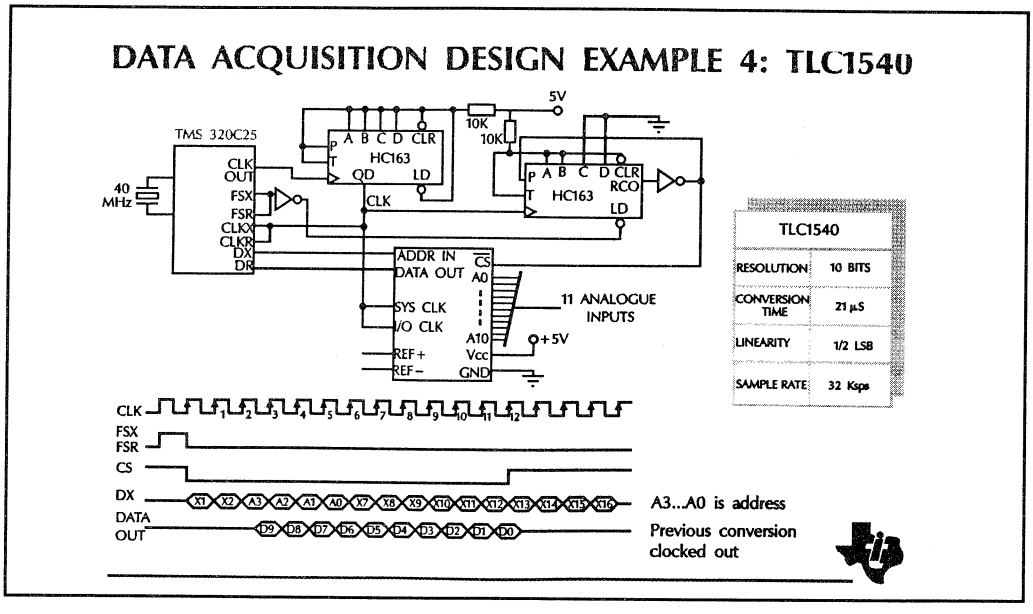


Figure 27 - The TLC1540 10 bit Successive approximation ADC

The TLC1540 is a successive approximation filter with 11 inputs and a serial output. This makes the interface to a TMS320C25 DSP with its serial input and output ports simple. The only external logic that is required is to generate the clock and timing signals and delays for correct conversion. In the diagram here it is shown operating in a mode with the system clock and I/O clock tied together.

TLC1540 10 bit Successive approximation ADC

O Full 10 bit resolution A/D converter
O Sample time ..... 5.5µs min typ
O Conversion time..... 21µs min typ
O Sample rate 32kHz
O Low power 6mW

This circuit uses synchronous counters to provide the I/O and SYS CLK signals for the TLC1540. With a 40 MHz crystal driving the DSP clock, the HC163 divides the CLKOUT output by 8 to produce a Clock signal at 625kHz , within the range of the TLC1540. The FSX

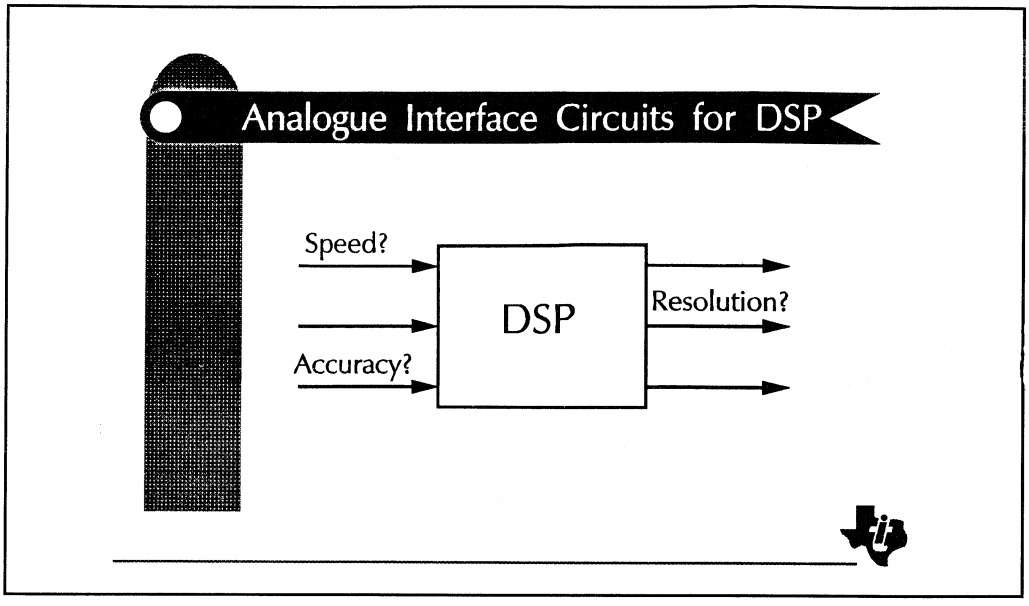
pin of the TMS320C25 is used to produce the chip select (CS) signal, which is linked to the CLK signals by the second HC163 synchronous counter. This is configured to give a pulse 12 CLKs wide allowing time to clock in the next address and to clock out the data from the previous conversion while CS is held low.

To provide noise immunity, the TLC1540 waits for 2 clock cycles after CS is taken low before accepting or outputting data. The Most Significant Bit (MSB) of the previous conversion is then placed on the data bus and the 10 bits are clocked out sequentially. At the same time , the address data is clocked in. The TMS320C25 uses 16 bit words, and so a 16 bit datastream is clocked out of the DX pin by the CLK signal into CLKR after the FSX handshake line has gone low. Since FSX is synchronised with the CS signal, and as we have seen the TLC1540 waits for two clock cycles after a change in CS, the address data must be placed in bits 3-6 of the data word as shown (A3...A0). This four bit address then selects the input channel required.

After the address is clocked in, the input signal is sampled via the selected channel during the next 6 clock cycles. At the end of this time, the result of the previous conversion has been clocked out. As CS goes high, the Data out line goes into a high impedance condition and the conversion process begins. Like most switched capacitor successive approximation converters, the TLC1540 has an inherent sample and hold function. During the sample phase, the internal capacitors are charged to the input voltage . Hence, this voltage is automatically held when conversion commences.

A further 44 clock cycles are required to complete conversion so that 56 clock cycles in total are needed for a complete access and conversion cycle. At 625kHz this corresponds to a total time of 90µS and a sample rate of 11kHz. The sample time is approximately 10µS in this example.

This concludes the section on design considerations with an example of an interface to a DSP. The importance of this area is such that the last section is devoted exclusively to it.



Section 4 - Analogue Interface circuits for DSP Applications

This section looks at the growing area of applications using Digital Signal Processors (DSP) as the "intelligence" in process control. These applications clearly require an interface between the digital and "real world" analogue signals. Texas Instruments has a number of devices designed to perform this task and they will be examined in the next few foils.

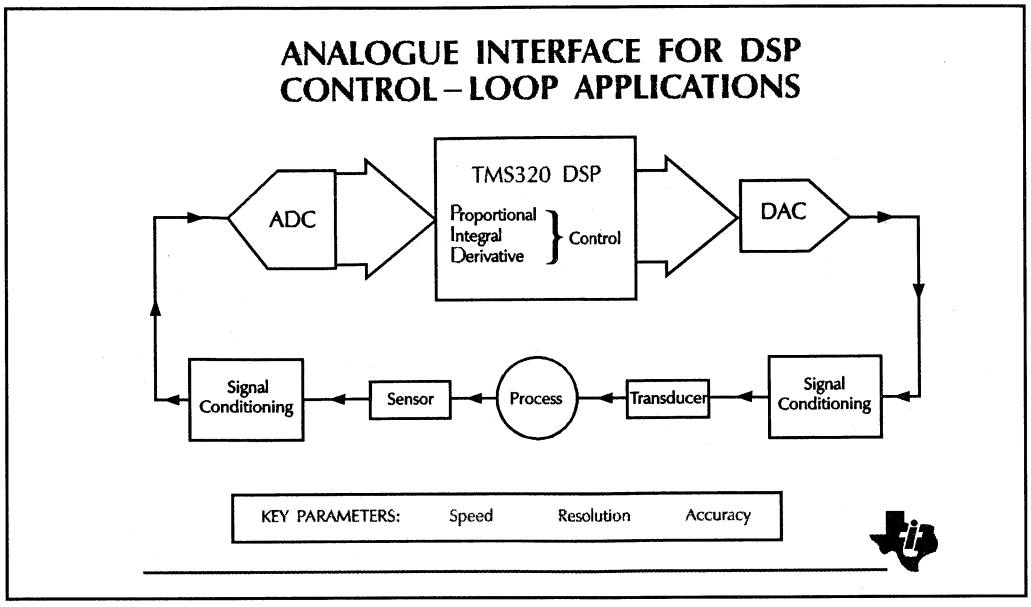


Figure 28 - DSP in process control

The use of a microcontroller or DSP as the core of a control system is a continuously growing field. As the cost of digital processing reduces, it becomes increasingly attractive for an increasing number of applications ranging from high speed digital processing for radar down to the control systems for white goods. To implement such applications , data conversion devices are required to capture data in its analogue form and convert it to binary digits, and then to take the digital control outputs and convert them back to an analogue signal to influence the process.

Such systems have requirements that impose conditions on the performance of the ADC and DAC; firstly there is the ability to capture data and make decisions in real time which dictates a certain minimum ***Speed*** requirement . The precision of control is decided by the ***Resolution*** of the converters and finally the accuracy of control is directly dependent on their ***Accuracy*** . These three parameters are the basis of any choice of converter for this type of application.

The diagram shows a system designed to operate using Proportional, Integral, Derivative (PID) control. In addition to the data conversion devices, there is a need for pre and post signal conditioning which usually takes the form of multiplexing, filtering and buffering the signals

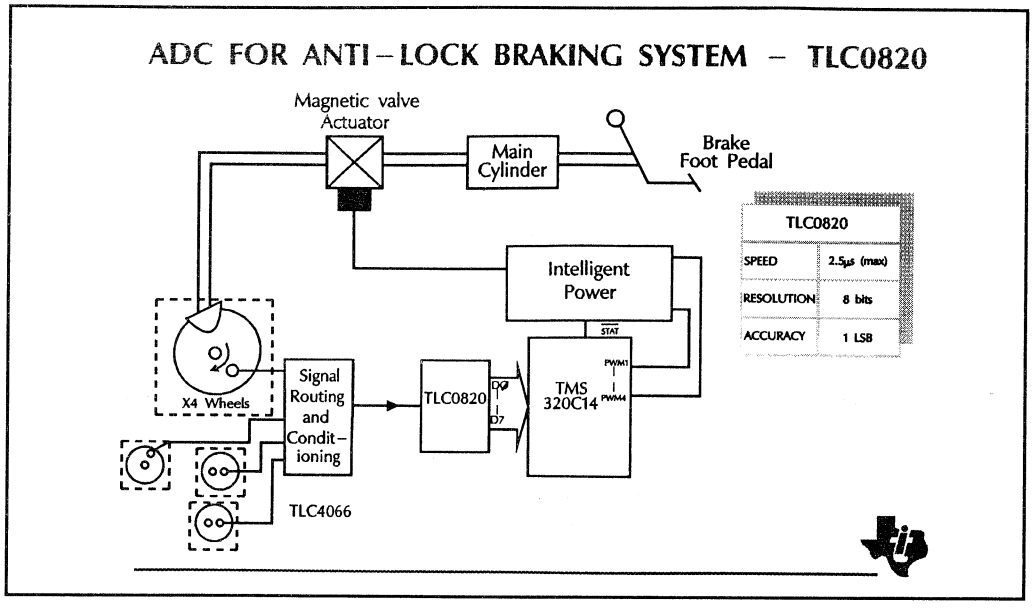


Figure 29 - An ADC for ABS systems

DSP solutions are being increasingly used in automotive applications. These include engine management, active suspension and the system featured here - an anti-skid (ABS) system. The automotive environment is electrically very noisy and the need for a high speed ADC is evident to ensure there is sufficient oversampling to extract the real signal from the noise. The basis of the ABS system is to ensure the wheels never go into a skid condition by monitoring their speed when the foot pedal applies the brakes ,and alternately applying and releasing the brakes under the control of the DSP . In this way, the wheel is prevented from locking up in a skid condition.

The speed of each wheel is monitored by a sensor that produces a pulse train in the range of 0 - 5kHz depending on the rotational speed. All four channels are routed together via a TLC4066 multiplexer which selects each signal in turn to pass to the ADC. High frequency noise is then removed by a Bessel LP filter which preserves the phase relationship of the signal. It is then fed to the TLC0820 ADC which converts the signal into 8 bit words . The primary factor in choosing this part is the speed of conversion required. In order to correctly reconstruct the underlying signal it is desirable to oversample at least 4 times. Hence , for 4 multiplexed signals operating up to 5kHz this gives

$$4 \times 5\text{kHz} \times 4 = 80\text{kHz} \Rightarrow 12.5\mu\text{S conversion time} \qquad 30.1.1$$

The TLC0820 has a semi-flash architecture which provides a conversion time of just 2.5µS max, so that it can operate in this system at up to 16 times oversampling if required. The semi-flash construction also provides a device with power consumption of just 75mW.

TLC0820 semi-flash ADC

O Conversion time 2.5μS max
O 8-bit resolution
O Total unadjusted error 1 LSB
O Single rail 5V supply
O Low power consumption .....50mW typ
O Differential reference inputs

Once converted, the binary data is processed by an advanced tracking filter in the DSP. This filter "tracks" the frequency of the input , to correlate it with an ideal pulse train at a particular frequency. In this way, it provides a "perfect" bandpass filter to determine the frequency and hence the speed of the wheel. Deviations from the desired control model are then measured and an output of PWM pulses is produced to control the length of time for which the brake should be applied. These are interpreted by intelligent power devices which provide the drive for the valve actuators that actually apply the brakes.

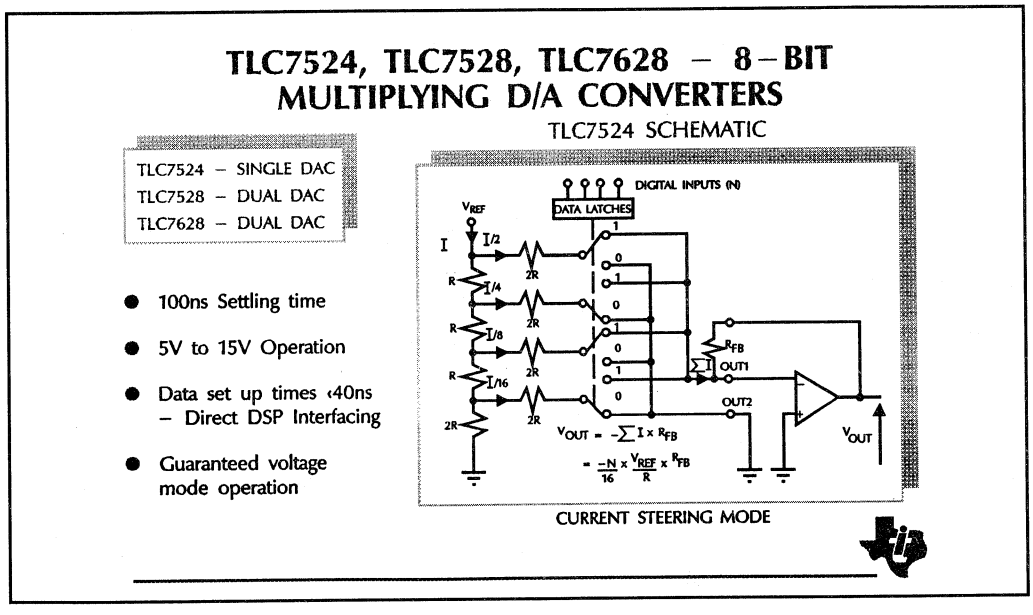


Figure 30 - TLC7524,TLC7528,TLC7628 Multiplying DACs

Many microprocessors operate with instruction cycle times that are too fast for direct interface to data converters. This
necessitates the use of buffer logic with increased costs in devices required and in board area used. The TMS320C25 with a 10MIPS rate (100nS instruction cycle time) is one such example of this. The TLC7524 DAC provides a solution to this problem with a settling time to 1/2 LSB of just 100nS. It can also be operated from a single 5V supply with a power dissipation of only 5mW.

The TLC7524 is a multiplying DAC fabricated in CMOS technology. The term "multiplying" comes from the fact that the value of the output is proportional to the input reference voltage multiplied by fraction of full scale represented by the input digital code. It uses an

inverted R-2R ladder to steer current from the reference input to the output via switches controlled by the digital input bits. This current output is changed to a voltage by an external op amp configured as a summing amplifier. However, this inverts the signal, so that this mode of operation requires a dual supply .

Also available in this family of devices are the TLC7528 dual DAC and the TLC7628 which is intended for applications running from a 15V supply but still requiring TTL level digital signals. Both feature excellant DAC to DAC matching so that they track together precisely.

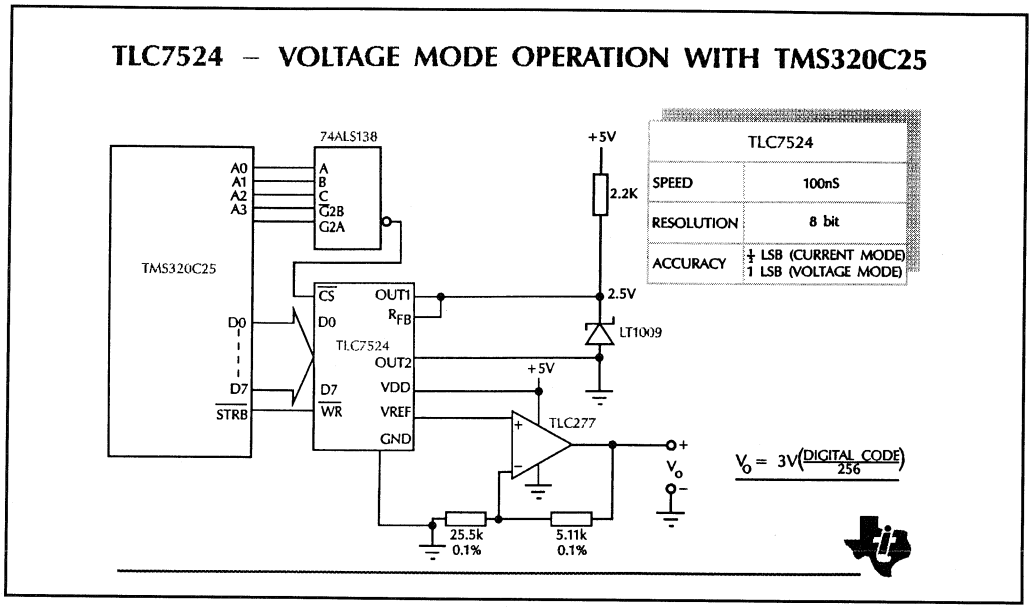


Figure 31 - TLC7524 - Voltage mode operation with DSP.

Single supply operation can be achieved by operating in voltage mode as shown here. In this configuration, the reference voltage is applied to the output pin OUT1 and the output is taken from the usual input pin V. In this mode of operation, the output is a voltage with the same polarity as the input so that single supply operation is possible.

TLC7524 multiplying DAC

O Settling time to 1/2 LSB....100nS max
O 8-bit resolution
O Linearity error 1/2 LSB
O Single rail 5V to 15V supply
O Low power consumption .....5mW max at 5V
O Guaranteed voltage mode operation

There are some points to note in this mode. Firstly, the impedance seen by the input voltage is not constant, but varies depending upon the input code. Therefore it is sometimes necessary to buffer the input with a voltage follower. In this case , the output impedance of the LT1009 is less than 1Ω so that it is not overloaded even under worst case conditions when the input impedance is 5kΩ. The LT1009 is chosen here for its high precision and low drift . Its

initial tolerance is +/-5mV at 25°C on a nominal reference of 2.5V, which is equivalent to 1/2 LSB.

Secondly, the switches in the DAC no longer have the same source-drain voltages, and as a result their on-state resistance is altered. This degrades the linearity of the part from the 1/2 LSB normally specified. Nevertheless, the device is guaranteed to meet 1 LSB linearity for an input of 2.5V at 5V V_{DD}.

The output is buffered and amplified by the TLC277 op amp which is chosen for its offset voltage of just 500µV max. The resistor chain provides sufficient gain to boost the output swing to 0V to 3V.

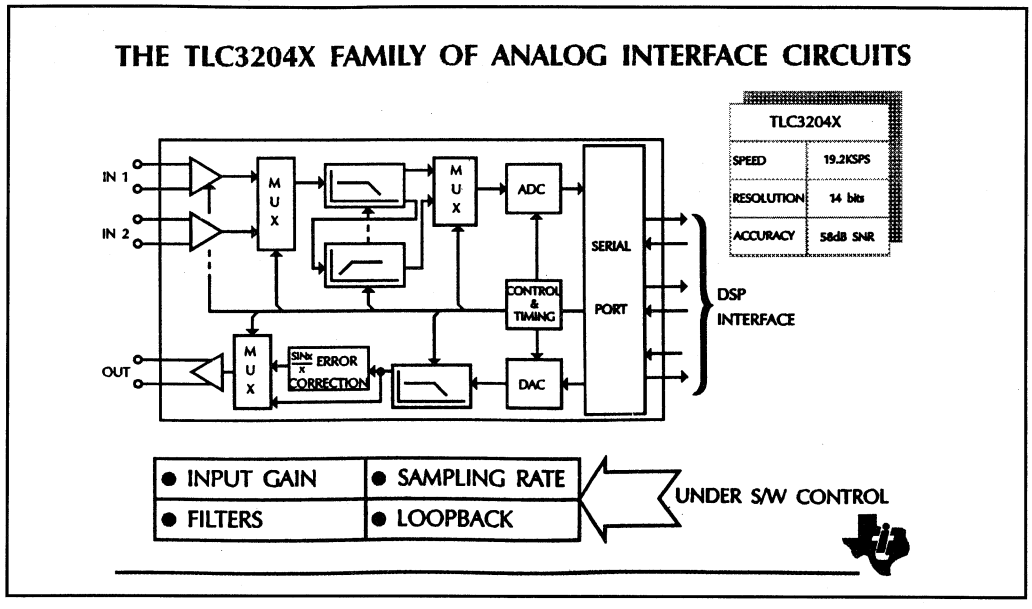


Figure 32 - The TLC3204X family of Analogue Interface Circuits (AIC)

One of the largest users of DSP based applications is in the Telecom segment of the market. This segment has clearly defined limits for the frequency of operation , with the audio band-width of up to 4kHz being the usual range of interest for the analogue signals.

To address the needs of this market, Texas Instruments developed the TLC3204X family of devices to provide the complete analogue interface for DSP in a single chip. All five members of the family are highly integrated with A/D, D/A, pre- and postfilter stages and an input/ output stage on-chip. They have been developed mainly for high performance voiceband system applications which require high resolution, a high degree of programmability , and an integrated design that conserves board space.

33.1 **AIC building blocks**

The AIC is divided into a transmit and a receive section which are controlled from a central timing block. On the receive side, an analogue signal is fed into either a main or auxilliary fully differential input which are selected by a multiplexer. The input stages have programmable gain so that the signal level can be optimised for maximum resolution. It is then passed to an antialiasing filter consisting of a LP followed by an optional HP which can be selected or bypassed as required. These are both switched capacitor filters (SCF) driven from a sub-multiple of the central master clock. This frequency is nominally set to 288kHz and all the

datasheet specifications are derived from this value, but it can be easily altered to adjust the corner frequencies of the filters.

The ADC itself is also driven from a further sub-multiple of the same clock which ensures the sampling is synchronised with the SCF filter. The sampling rate is programmable up to 19.2kHz , and encompasses the standard modem sampling rates (7.2kHz, 8.0kHz, 9.6kHz , 14.4kHz). The output from the ADC is a 14 bit word which is then passed out of a serial port to a DSP.

In the transmit section, data and control information is transferred from the DSP into the DX pin of the serial port. This is transmitted to a 14 bit DAC which is controlled in the same way as the ADC. The sampling rate for both can be tied together in ***Synchronous*** operation but they can be run independently in ***Asynchronous*** mode. The output from the DAC is fed to a LP SCF and then to a SinX/X correction filter . It is finally transmitted out of a differential output buffer.

TLC3204X AIC

O 14 bit ADC and DAC
O Programmable sampling rates up to 19.2kSPS
O Programmable switched capacitor filters
O Direct serial interface to DSP
O Synchronous and Asynchronous operation

The advantage of using the AIC in a system design , is the degree of flexibility that results because parameters can be controlled by software and do not require costly hardware modifications. Applications like a facsimile and a secure telephone both dictate a high speed data rate with low bit error rate figures (BER). This in turn demands a flexible system with high
resolution. Both these parameters are met by the AIC with its 14-bits of resolution and up to 19.2 Ksamples/s data rate.

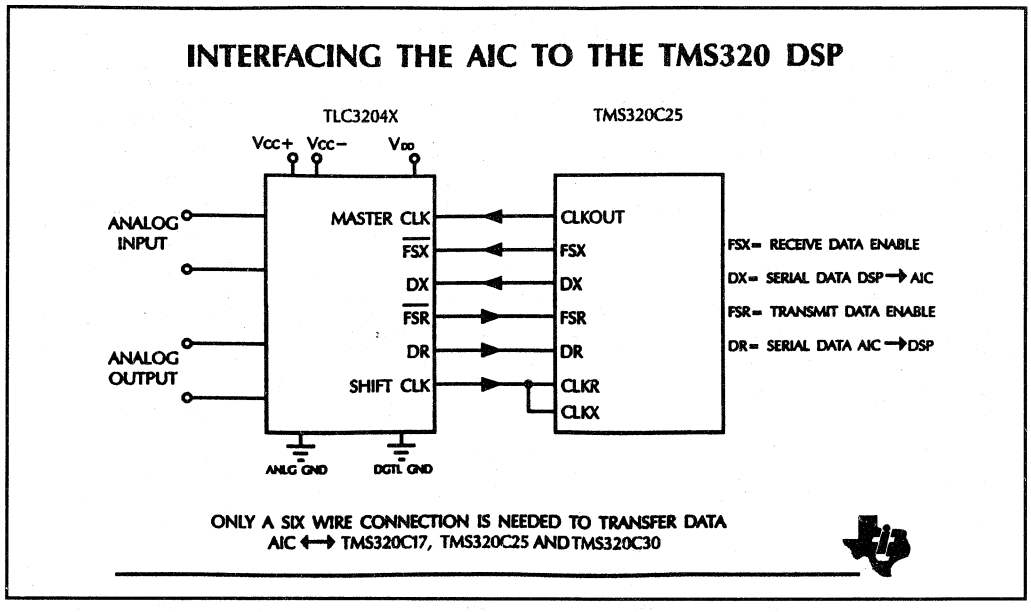


Figure 33 - Interfacing the AIC to the TMS320 DSP

The interfacing part of the AIC is built on a serial data format concept aimed at interfacing the device directly to the serial I/O of the TMS320C25 digital signal processor. As such, the core of the system consists of these two chips alone, rather than being supplemented by a number of interface devices commonly found in many applications.

The intercommunication between the AIC and the DSP is based on just six lines. These are outlined in the following list

MASTER CLK : The AIC is built on a single master clock input which is divided by the contents of control registers to determine the conversion rates and filter characteristics.

FSX : Initiates the AIC to prepare for a data transfer from the host processor.

DX : When the FSX has initiated the AIC,a transfer of data will take place to the AIC from the host along this line.

FSR : Initiates the serial input of the host to receive output data from the AIC.

DR : When the FSR serial input has been activated, the AIC will transfer data from the A/D to the host along this line.

SHIFT CLOCK : Dictates the speed of data transfer between the AIC and the host.This clock shifts the data into and out of the AIC.

SUMMARY

		TYPE	COMMENT	APPLICATIONS
ADCS	TLC7135	Dual slope	14 bit resolution	DVM, strain gauge
	TLC1125	Successive approximation	12 bit, self calibrating	Process control, modems
	TLC1540	Successive approximation	10 bit, ½LSB linearity	Control, DSP interface
	TL5501	Flash	6 bit, 20 MSPS	Scanner, video
	TLC0820	Semi-flash	8 bit, 2.5μs conversion time	ABS
ADC+DAC	TLC3204X	Successive approximation	14 bit resolution, 58dβ (SNR)	Modems, speech
DACS	TLC7524	Multiplying	8 bit resolution, guaranteed Voltage mode operation, interface to μp	Process control, DSP interface
	TLC7528	Multiplying		
	TLC7628	Multiplying		
	TLC5602	FLASH	8 bit, 20 MSPS	Video
SCF	TLC04	4th order Butterworth	Cut-off frequency 0.1Hz to 30KHz	General purpose filtering
	TLC10	Dual 2nd order variable	Configurable filters, Cut-off frequency up to 30KHz	Anti-aliasing

SECTION 4.
DATA TRANSMISSION

DATA TRANSMISSION INDEX

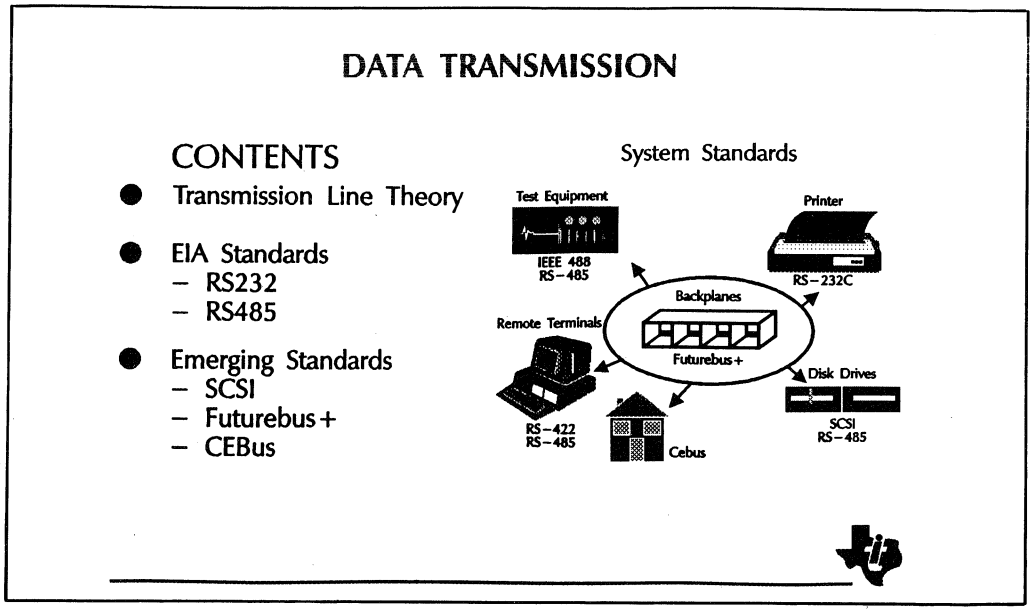


Figure 1 - Data Transmission

The following sections focus on a range of data transmission products supported by the Linear Department of Texas Instruments.

The range of products discussed are characterised by yielding greater current output drive capability and/or a wider output voltage range than that normally found in standard TTL type devices. As a consequence the application areas discussed involve the transmission of digital data over long distances and usually in electrically hostile enviroments.

In addition several of the new emerging standards are discussed. These too are demanding applications which require the design expertise and technologies available to Texas Instruments Linear Department.

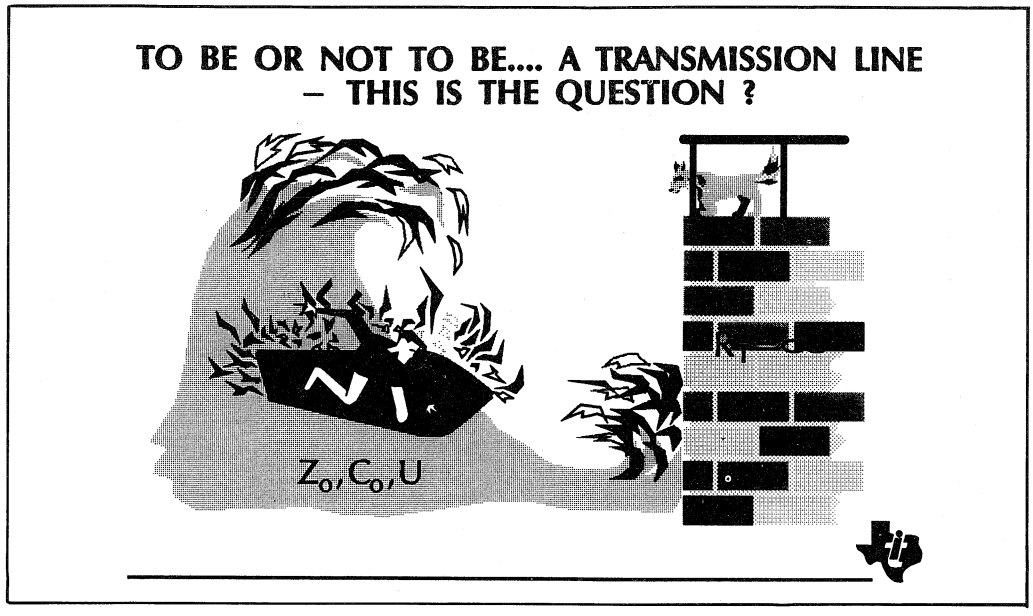


Figure 2 - Transmission Line Theory

Before studying the more practical considerations of implementing a digital data link an understanding of the signals behaviour is needed. More specifically a method of identifying potential problem areas and how to overcome them is necessary. This is dealt with very briefly in the following section.

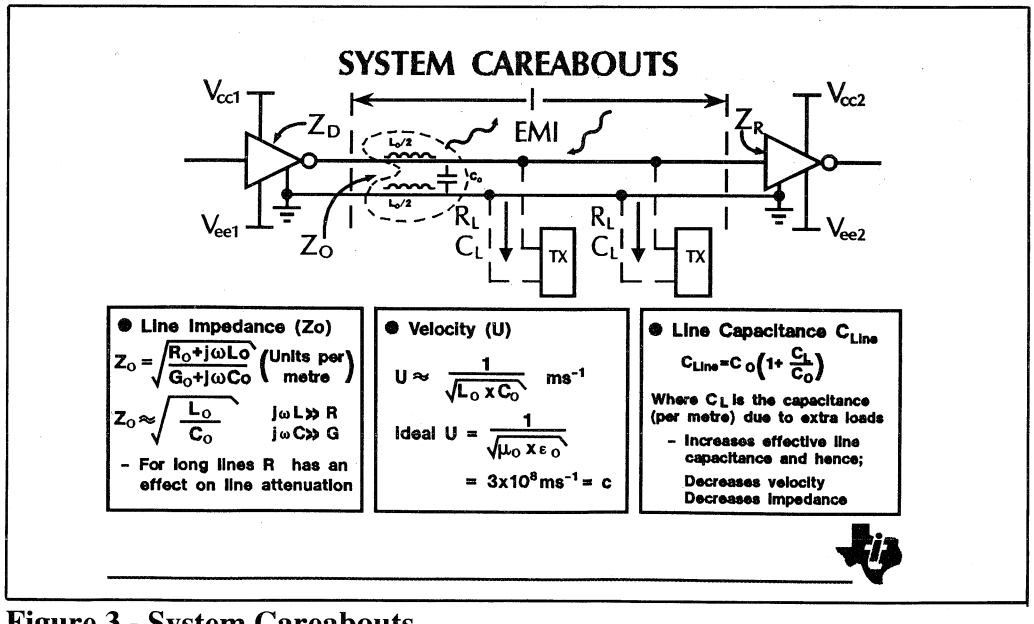


Figure 3 - System Careabouts

Digital communication within a system could, for instance, be divided into three different areas. The transmission of digital data from one integrated circuit to another on the printed circuit board. The transfer of data between circuit boards via the system backplane.

The transfer of data between separate equipments or peripherals over still longer distances, for example by using RS485 links.

In the first two instances, data transfer on printed circuits and along backplanes usually takes place with TTL or CMOS logic level signals. Even so, the speed of the backplane system will be slower than that of the printed circuit system simply because of the differences in electrical characteristics of the printed circuit track and backplane wiring. These differences in electrical characteristics become even more conspicuous when using high speed long distance communication links such as RS485.

At low data rates we can treat a cable as a pure short circuit, and assume that the propagation delay of the signal along the cable is negligible and does not impact on the overall system performance. However as data rate and distance increase then the speed and shape of the data signal will start to be governed more by the electrical characteristics of the cable, such as its capacitance, inductance and resistance. This will lead to a certain amount of degradation of the signal quality. Not only does a signal degrade due to the electrical properties of the cable, it also suffers degradation from external sources of interference. It is obvious therefore that these limitations should be comprehended into the design of a digital data communications link, after all a cable is not always "just a piece of wire".

As a final note, it should be emphasised that the problems encountered with digital signals on printed circuits and backplanes are exactly the same in nature as those encountered with the comparatively long distance systems that we are discussing here. In practice though, the digital design engineer is often better equipped to deal with the former class of problem.

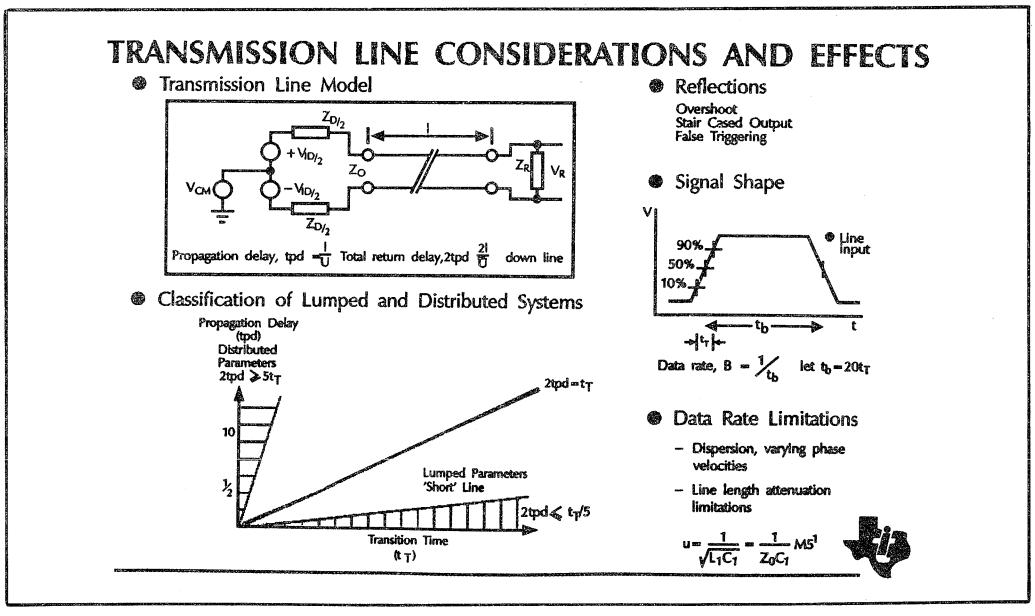


Figure 4 - Transmission Line Considerations and Effects

Having reviewed the external influences on data integrity lets now discuss how the signal itself behaves during transmission. Only when this has been done can a decision as to whether the line should be treated as a lumped parameter line or as a true transmission line be made.

A transmission line differs from a lumped parameter model in that it models the connecting circuit in terms of distributed parameters (inductance, capacitance, resistance, conductance), rather than as an equivalent lumped load on the line. The transmission line can be considered in terms of an infinite number of small filter sections making up the line. The result is that a transmission line is said to have a characteristic impedance, Z_0, which is independent of distance along the line and represents the voltage and current relationship for a wavefront at any point as it travels along the line.

The transmission line will always consist of two conductors. The current will flow in opposite directions in each of the conductors. In the single ended case, one of these conductors is the ground wire.

The speed that a pulse travels at along a transmission line approaches that of the speed of light. The limit to the actual speed will very much depend on the type of cable used.

All cables can be thought of as transmission lines; but the term, transmission line, is used with differing meanings. If the signal starts to change at the transmitter output at one end of the line, the effect of this change will eventually be seen at the other end of the line. A reflection of the signal will occur, which will eventually return back to the transmitter te rminals. If this happens before the original transmitted signal has risen to its peak value then the line will normally be treated as a lumped parameter system rather than as a true transmission line. This is because the line itself is not really seen to be greatly influencing the performance of the system. A general rule of thumb for determining if a system should be treated as a true transmission line can be formulated. If the risetime , t_t, of the signal is much less than the round trip propagation delay, $2t_{pd}$ of the signal from transmitter to receiver and back to transmitter, then the cable can be treated as a transmission line and not as a lumped parameter model. A better model is given by allowing 10 one way propagation delays, t_{pd} to occur during the transition edge time.

When the cable is operating like a transmission line, extra loads in the form of transmitters and receivers can be added , providing that they do not cause too great a shunting effect on the line. These extra loads, if they are evenly distributed along the line, can be treated as an extra distributed capacitance along the line adding to the effect of the line capacitance and inductance. The extra devices will decrease the line impedance and reduce the speed of the signal along the line.

If the cable cannot to treated as a transmission line, then a lumped paramter model would consider the line to represent a pure fixed load to the transmitter device. For example, the capacitance of the line will be modelled as a fixed value which effectively limits the output voltage slew rate of a transmitter device that can supply a finite amount of current to the line.

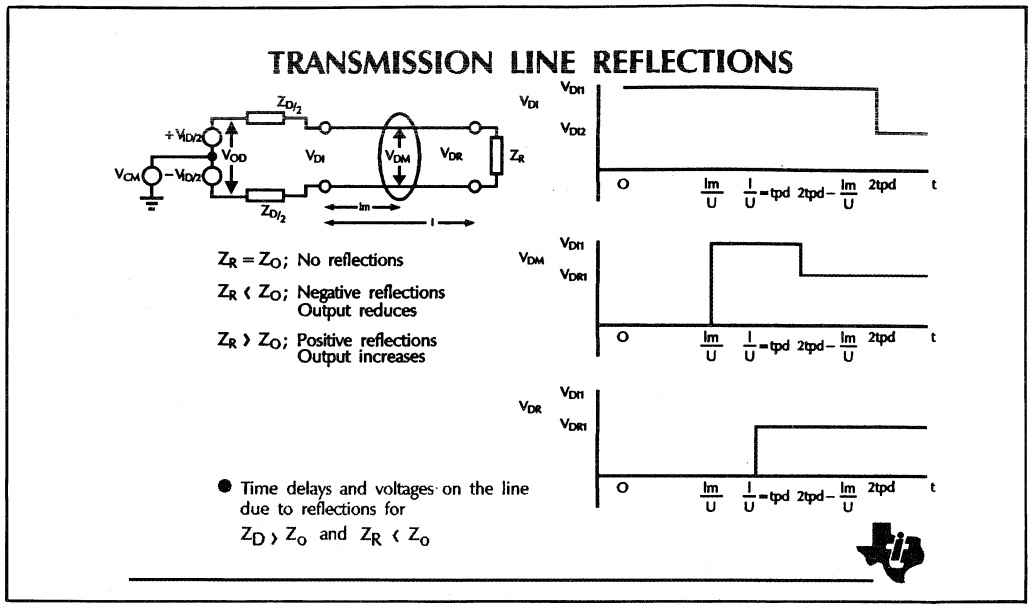


Figure 5 - Transmission Line Reflections

Imagine a driver circuit driving the line. When the driver output changes state, the driver appears to see the effective characteristic impedance of the line, Z_O . This will cause the voltage at the output of the driver circuit to drop as a result of the potential divider formed by Z_O and the driver circuit output impedance, Z_D.

It is useful to consider that at any point along the line, the source impedance will appear as Z_O, and the load impedance will also appear as Z_O. This gives the impression that the line is being driven by a voltage source, V_{IE}, of twice the magnitude of the line voltage.

If when the signal reaches the receiver end of the line it sees a receiver impedance equal to the impedance of the line that it is already travelling on (Z_O), it will tend to interpret this as a continuation of the line. The voltage on the line will not alter and the current flowing along the line will flow through the termination resistor and back to the driver via either ground or the other line in the system. Operation of the circuit as just described would result in optimum data transmission efficiency, with little or no signal reflections. However, circuit operation in the real world is not always so perfect.

If the termination impedance is not similar to the characteristic impedance of the line itself, the voltage at the termination point will alter. The voltage at the termination point is dependent on the relative size of the termination impedance to the line impedance. If the termination impedance is higher than the line impedance, the line voltage will increase causing a positve voltage reflection of the signal. When the termination impedance is lower than the line impedance, the line voltage will decrease leading to a negative reflection. The same effect will occur at the driver output terminals due to impedance mismatches between driver and line..

Reflections at each end of the line will eventually settle and leave a constant d.c. voltage on the line. The value of this voltage is equal to the ideal open circuit output voltage multiplied by the termination impedance divided by the sum of the driver output impedance and

termination impedance.

Reflections as described can cause problems when driving lines at high frequencies. False triggering of the receiver can occur, and the repeated signal reflections mean that signal waveshapes are distorted.

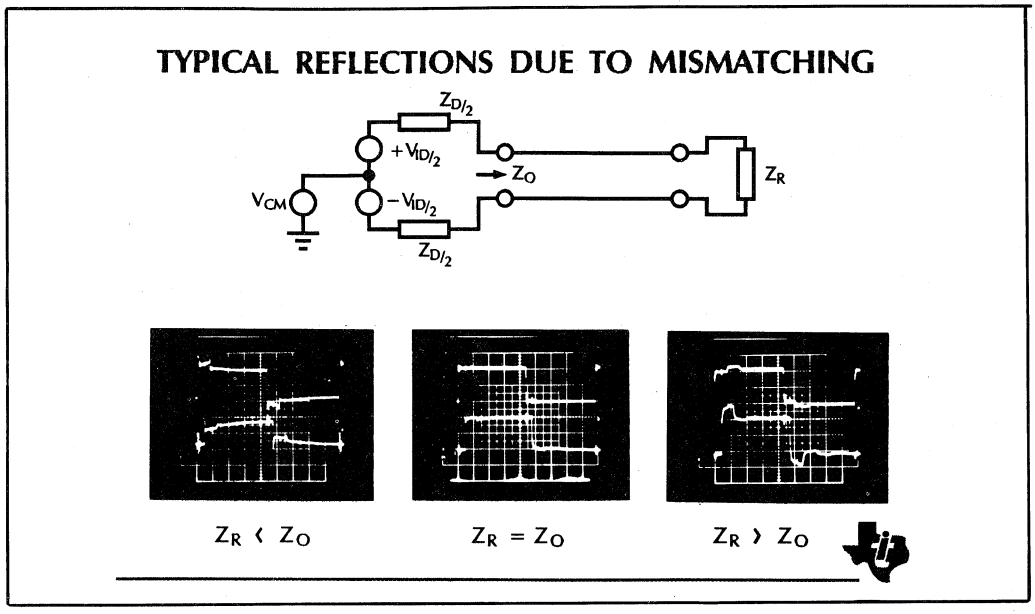


Figure 6 - Typical Reflections Due to Mismatching

The theory developed previously is now shown in practice.

For $Z_R<Z_O$ is can be clearly seen that the incident wave (top trace) is reduced by the reflection voltage.

Similarly the reflection voltage is seen aiding the incident voltage for $Z_R>Z_O$ The ideal condition, $Z_R=Z_O$, produces an incident voltage which is relatively free from reflection voltages.

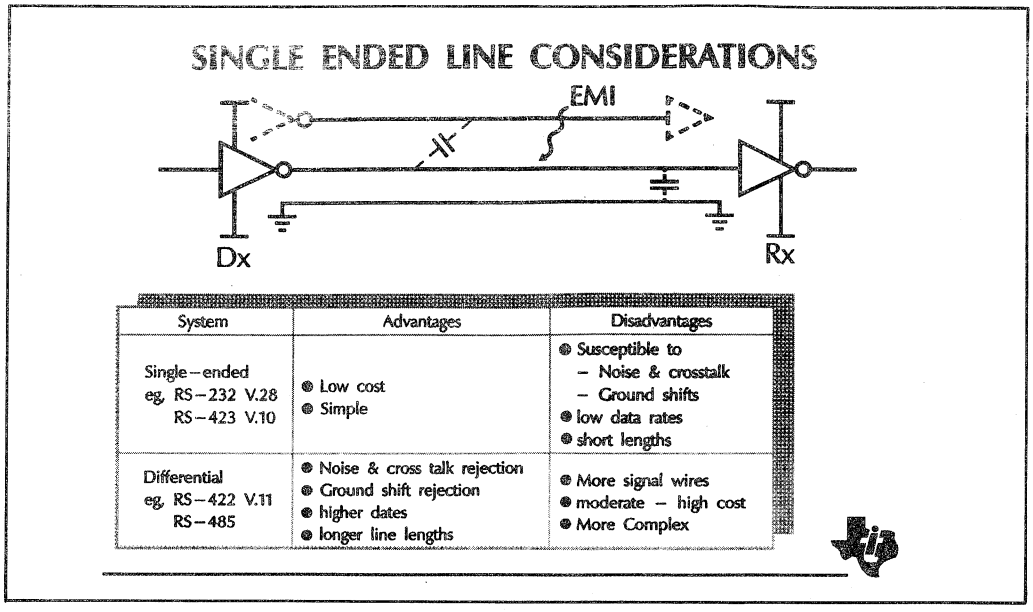


Figure 7 - Single Ended Line Considerations

Single ended data transmission systems consist of a signal line which the data is sent down and a ground line through which the current returns. A direct result of this is that the ground line is part of the transmission line, which can be of benefit in some circumstances but not in others.

One of the major benefits, and most obvious, is that a single ended system is the cheapest solution in terms of cabling costs. In general terms it requires only half the cable of a differential system. It is also relatively simple to install and operate.

The main disadvantage of the single ended solution is its poor noise immunity. Because the ground wire actually forms part of the system, if there are any spikes or shifts induced into it (from nearby high frequency logic or high current power circuits), then the net effect is that erroneous data is received. For example, a shift in the ground potential at the receiver end of the system can lead to an apparent change in the input switching threshold of the receiver device, thus increasing susceptibility to noise. Another common problem area with single ended systems is the effect of crosstalk between adjacent signal lines and the coupling into the line of noise from other sources. The line is both inductive and capacitive and so will be susceptible to both electrostatic and magnetic coupling.

The crosstalk pick-up in the line is related to the effective coupling capacitance and the terminating impedance of the line. The higher the impedance of the termination circuit, the greater the induced voltage due to crosstalk. The induced voltage due to crosstalk also increases as the frequency or edge speed of the crosstalk signal increases.

These problems will normally limit the distance and speed of reliable operation for a single ended link.

The induced noise can be reduced by:-

i) Limiting the slew-rate of signals so that they do not cause crosstalk to be induced onto other lines.

ii) Limiting the line length.

iii) Shielding the signal conductor.

While the system noise could be reduced by:-

i) Isolating the signal ground from power conductors. (E.g. keep signal grounds separate as far as possible from power grounds.)

ii) Ground wires should be as low as impedance as possible.

iii) Use star ground system configurations

Some of these techniques are used in systems such as RS-232 and the forthcoming Futurebus backplane system, which limit the slew-rate of signals by capacitive means (RS232) and by intentional generation of trapezoidal signals (Futurebus).

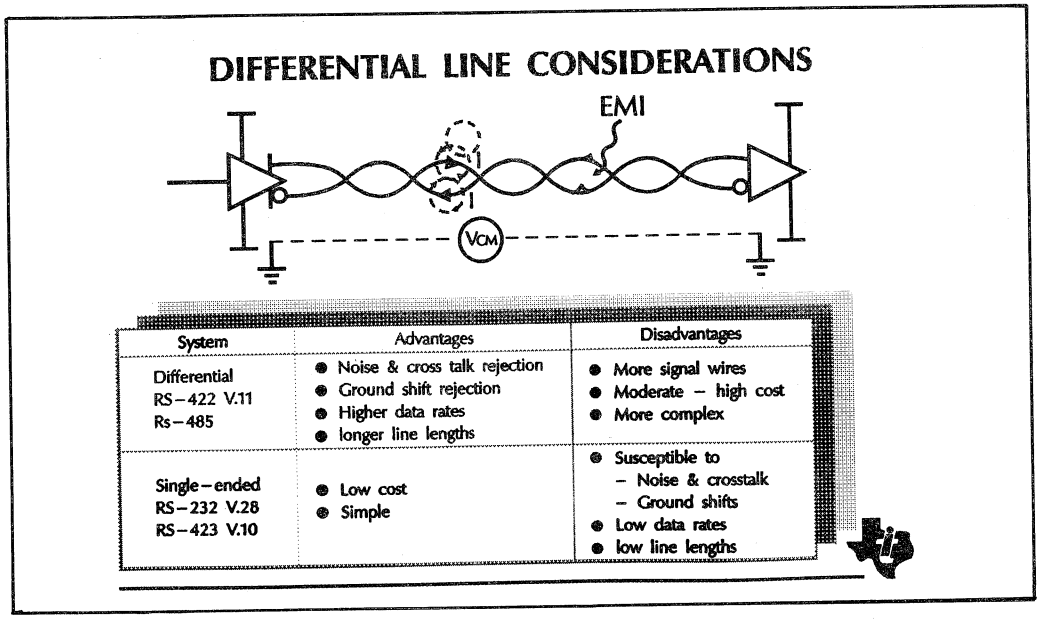


Figure 8 - Differential Communication Lines

A differential communication system involves the use of two signal carrying wires between transmitter and receiver, such that the signal current flows in opposite directions in each wire. The net effect of doing this is that the receiver is only concerned with the *difference* in voltage between the two wires. The absolute value of the d.c common mode voltage of the two wires is not important. In practice, transmitters and receivers have a finite common mode voltage range in which they can operate.

The use of a differential communications interface allows transmission of higher data rates over longer distances to be accomplished. This is because the effects of external noise sources and crosstalk effects are much less pronounced on the data signal. Any external noise source coupling onto the differential lines will appear as an extra common mode voltage which the receiver is insensitive to. The difference between the signal levels on the two lines will therefore remain the same. By the same arguement, a change in the local ground potential at one end of the line will appear as just another change in the common mode voltage level of the signals. The differential output to the line will also provide a doubling of the driver's single-ended output signal. Twisted pair cable is commonly used for differential communications since its twisted nature tends to cause cancellation of the magnetic fields generated by the current flowing through each wire, thus reducing the effective inductance of the pair.

The main disadvantage of a differential system lies in the fact that two cables are required for each communication link. This increases system cost, but provides superior performance when data is to be transmitted at high rates over a long distance.

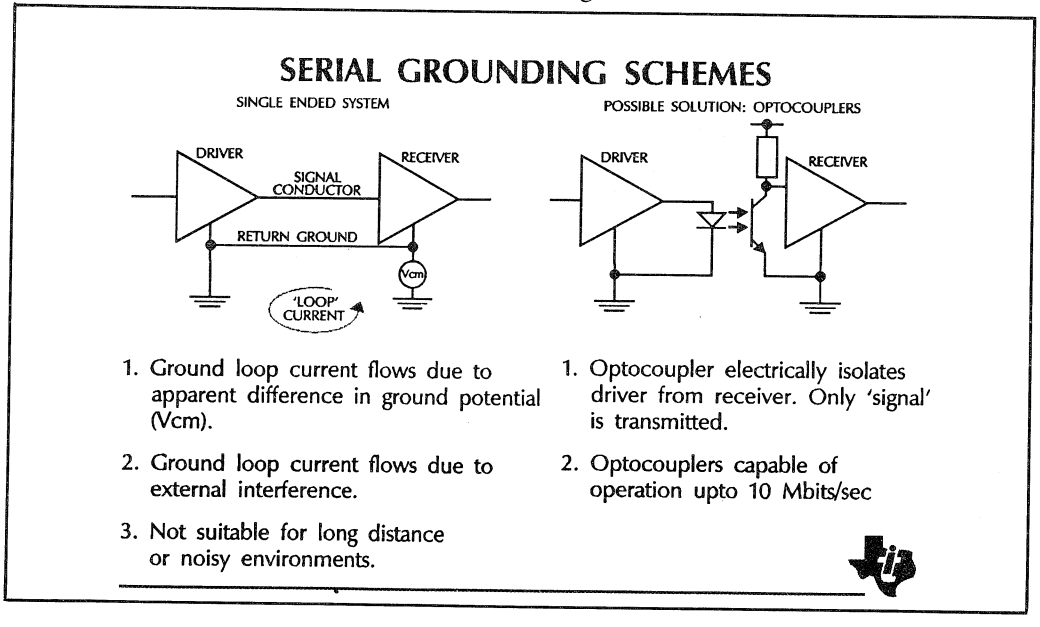


Figure 9- Serial Grounding Schemes

Setting the Scene

Grounding should be considered early in the design phase of a party line system, there now follows a brief discussion of the grounding considerations.

A 'ground' is an assumed arbitrary point of zero potential, and a ground connection is a tie to a point as close as possible to a ground potential. The objective of any grounding technique is to provide a path to earth of as low a resistance or impedance as possible . The reason for this is quite clear , the flow of current causes a voltage drop that is directly proportional to the resistance of the path to ground. Any resistance that results in unwanted difference of potential is the source of coupling to other circuits. The above may seem obvious but it emphasises the

importance of principles like single point grounding in high performance linear circuits and the need to seperate 'noisy' digital grounds from 'quiet' analogue grounds in a circuit. Of course the analogue and digital grounds will have to be commoned at some point in the circuit, the terminals or at the zero volt bus bar for example.

Single Ended Transmission

For single ended data transmission it should be possible to transmit the data along a signal conductor to the receiver and then return the current to the zero volt potential. In ideal circumstances, the 0V connection at the driver and receiver devices should be at the same potential. However in long line applications , what often happens in practice is that there is an apparent change in local ground or 0V potential at one end of the system. This is represented on the foil by Vcm in series with the receiver ground. Vcm will cause the incoming signal to appear to have a reduced common mode voltage (assuming Vcm is positive). Vcm can reach values of several volts which could cause the link to fail. For example, if the receiver input switching threshold was set at 1V and Vcm was 5V, then the incoming signal would need to have an effective value of 6V just reach the receiver's input switching threshold.

An obvious way to prevent the situation just described is to ensure that both receiver and driver have a common ground reference. This can easily be achieved by connecting a signal return/common ground wire between driver and receiver. However doing this can introduce another problem known as a 'ground loop' or 'earth loop'. This is formed because current is now free to flow as shown in the loop made up from the signal return wire and the earth path. Since Vcm is in this loop, current flows. If the loop encompasses many pieces of equipment, then the net result is that each equipment ground (or I.C. ground) will have a different potential (something to be avoided).

In addition to the ground loop current that flows due to differing ground potentials, inductive coupling of signals external to the circuit into the ground loop is also another area of concern. The ground loop is prone to this effect since it forms a loop of large area and low impedance and is therfore highly inductive. In low frequency voice grade circuits, the interference is commonly found in the form of a.c. hum picked up from nearby power supplies.

Therefore single ended communication is not recommended for use in noisy environments due to interference coupling or for use over long distances if there is a possibility of ground shift.

A more complete solution to the problem of ground shift and interference involves the use of optocouplers in order to electrically isolate the output of the driver from the receiver input. This is shown in general form on the foil. Since there is no electrical connection between driver and receiver, then no earth loop is formed. Modern optocouplers also have extremely good rejection capability to high frequency common mode signals; as high as 10kV/ms and can operate at upto 10Mbaud (HCPL2601 from TI).

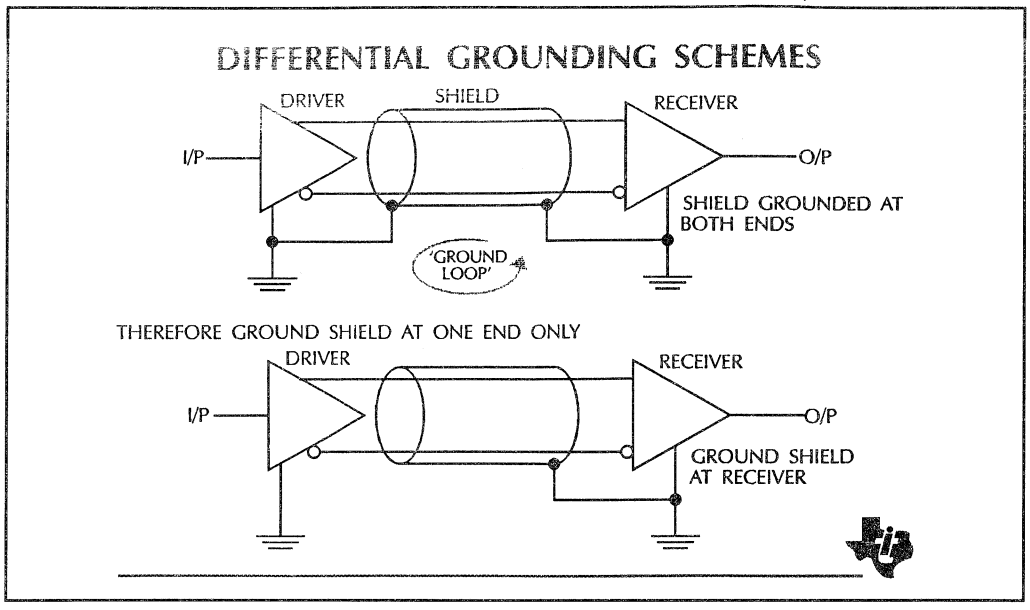


Figure 10- Differential Grounding Schemes

This foil illustrates a very simple guideline for dealing shield grounding in differential systems. If the shield is grounded at both driver and receiver ends, then a possible ground loop path exists which can lead to problems already described.

The answer is to ground the shield only at the receiver end. This ensures that a ground loop current cannot flow. The shield therefore acts as a low impedance path to ground for externally interferring signals.

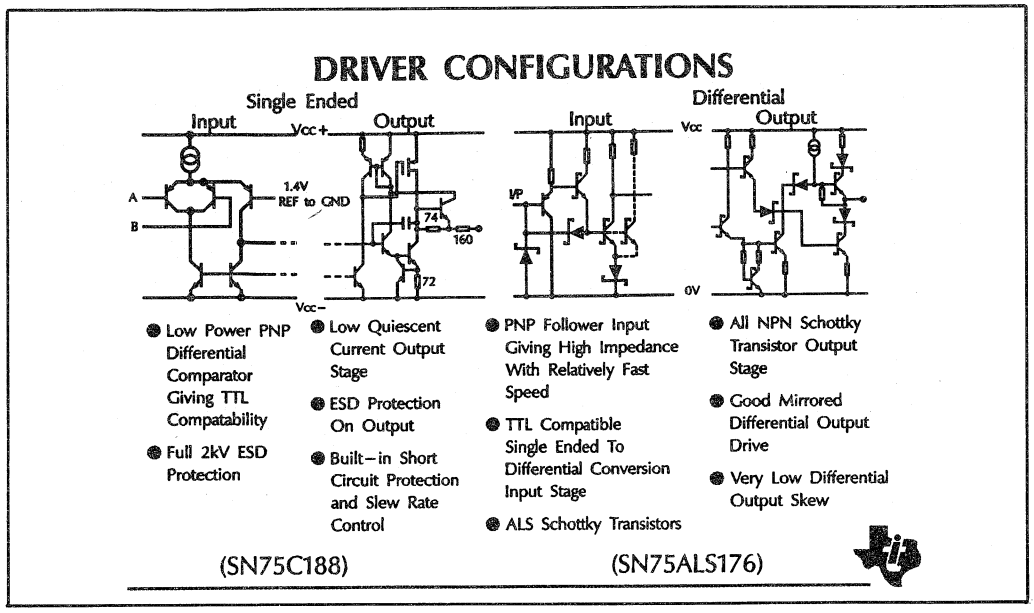


Figure 11 - Driver Configurations

The two basic formats for data transmission systems; single ended and differential, have differing current and voltage requirements. As a consequence there are differences in the internal structures of the semiconductor integrated circuits that are used to drive lines in each of the two formats. The biggest difference lies in the design of the output stage circuitry of the devices.

Until recently, the semiconductor technologies used to manufacture line interface circuit devices have all been based upon those technologies and processes used to build digital logic circuits. This resulted in circuits having mainly bipolar NPN structures. For example the change from ordinary bipolar to low power schottky (LS) advanced low power schottky (ALS) technologies in digital logic devices, was closely followed in line circuit devices.

In recent years though, there has been a change in the digital logic field towards device structures based upon CMOS processes. CMOS offers the obvious attractions of low quiescent power consumption and operating speed comparable to that of many bipolar technologies. The same change in technology for line circuits has not been so fast. One of the primary reasons for this is the need to make output transistor stages very large in CMOS technology to enable them to source the required high currents (as much as 250 mA). The input capacitance of these large CMOS stages also require much higher drive currents from the bias circuits. At high frequencies of operation CMOS line circuits therefore lose some of their attraction because bias currents become so high. It is also difficult to build CMOS devices that could withstand the relatively high voltage levels used by some slower, older line interfaces, for example RS232.

The most promising route forward in technology for line interface devices would appear to be through the use of a BiCMOS technology. Such progress has again already been made in the digital logic field. BiCMOS technology combines the speed and high voltage capability of bipolar processes with the low supply currents and high input impedances of a CMOS process.

Consideration of the circuit schematic for the input stage of most line driver circuits will show them to be TTL compatible. The SN75C188 quad RS232 driver and SN75ALS176 RS485 transceiver demonstrate this. The inputs of both devices feature a reversed bias diode and resistor to the positive supply and an effective two forward diode drops to ground. This is a similar configuration to that found in a standard TTL gate and results in the 0.8V and 2.0V TTL threshold levels. However, the SN75C188 has been designed for dual rail applications and so shifts the 0-5 V input voltage to the +/-12V output voltage range. Since it is designed to drive differential lines, the SN75ALS176 includes a single to differential converter stage consisting of a latch with an extra inverter structure.

Single ended line drivers are normally used to transmit data at lower speeds and require less output current drive capability They are therefore good candidates for implementing in a lower power process technology. An new generation of RS232 devices built using a BiMOS process has emerged to make low power consumption a reality. The new Generation of low power BiMOS devices includes quad drivers and receivers (SN75C188/198/189), both triple and quad combined driver/receivers (SN75C1406/1154) and a mixed three channel driver and five channel receiver (SN75C185).

The new BiMOS technology devices offer more advantages than just reduction in power consumption; slew rate limitation of the RS232 signal to 30V/us is carried out on-chip. This obviates the need for external capacitors.

Another feature which has been introduced to single ended systems such as RS232, even though they were never intended to be used in such a manner, is the capability to disable the output from the line. This is possible with the SN75C198 and LT1030 quad line drivers. This has a major effect in saving the standing current that normally flows in the RS232 line.

High speed differential output drivers, the SN75ALS176 for example, use an all schottky npn totem-pole output stage. This increases the output switching speed performance over technologies using pnp transistors in critical signal paths. The advanced low power schottky technology (ALS) also substantially reduces supply current consumption over standard LS npn structured devices (SN75176).

As the data rates demanded from systems increase, switching speeds in differential driver outputs also increase. However, since the outputs are complementary in nature, it is essential that the two outputs change state at the same time. Totally simultaneous switching when driving a long cable is almost impossible to achieve, but the excellent signal skew specifications for 'ALS devices make them suitable for the most demanding applications, SCS1, IPI for example.

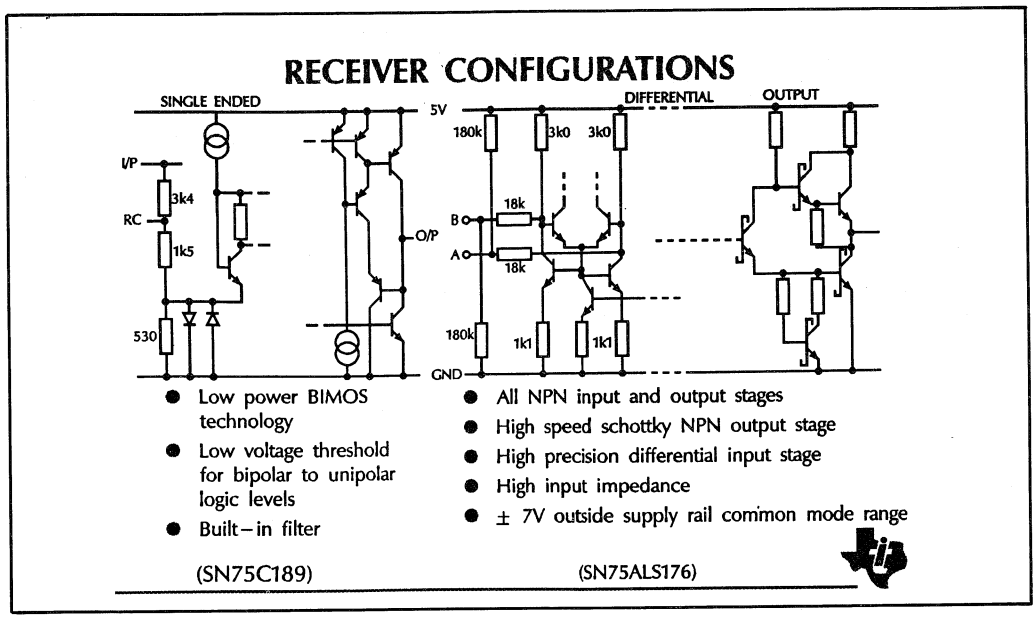


Figure 12 - Receiver Configurations

The design of a line receiver circuit is also dependent upon the type of data transmission system it is ended to work in. The key operational parameters to be specified include:

i) Differential or single ended inputs.

ii) Input signal switching threshold.

iii) Input signal common mode range.

iv) Speed/power requirements.

The design of a single ended receiver is usually simpler than that of its differential counterpart. The signal input stage to a single ended receiver is similar in function to a voltage comparator circuit. The input signal is compared to an internal reference and the output switched accordingly.

New generation RS232 receivers, constructed using BiMOS technology, have been designed to meet new systems' power saving requirements. They also include line noise rejection filter circuits in their design, providing further system integration. The filters incorporated into the receiver are capable of rejecting voltage noise and glitches on the line which are less than 1us duration. This feature saves on board space and reduces external component cost. The output stage of the SN75C189 receiver circuit has been designed using a low power common emitter circuit.

Differential receiver circuits have to operate in the presence of large common mode d.c. voltages at the input terminals, while still maintaining a good differential accuracy. This is achieved by making the heart of the receiver a high speed differential amplifier. The common

mode range of this amplifier is small, so as to maintain its gain accuracy and speed. However, in order to cope with the large common mode input voltages, from -7V to +12V, the input circuitry incorporates a potential divider network that reduces the effective common mode input voltage while still maintaining a high input impedance. The network clamps the common mode part of the signal to a constant level suitable to the differential amplifier stage. The same resistive network also provides the large minimum input impedance required to meet RS485 requirements.

The output stage of these receivers uses an ALS npn transistor network which provides the high speeds demanded by the RS-485 system, while maintaining a good power consumption at these speeds.

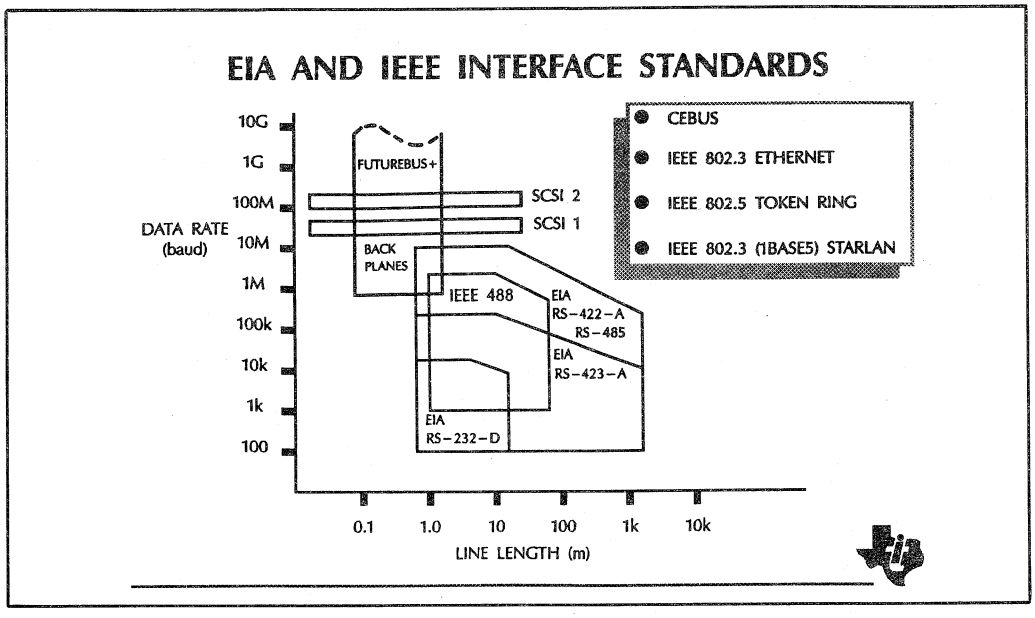


Figure 1 - EIA and IEEE Interface Standards

Data transmission circuits are chosen primarily on the distance and data rate and distance to be covered. Compliance with industry standards is necessary to maintain system compatibility. Standards vary in line length and data transmission rates to achieve the desired performance as shown, and are classified by their application and what they interconnect.

The backplane or boardlevel bus is the most general and widely used of the parallel bus types. Examples are the microprocessor specific Multibus and VMEbus. However, increasing need for even higher backplane data rates and optimised flexibility without being tied to a specific microprocessor architecture is solved by the rapidly emerging standard - FutureBus+. SCSI (Small Computer System Interface) is also a parallel bus structure with expanding use for the particular application of data transfer between PC/Workstations and memory storage systems including winchester disk drives.

Finally, IEEE488 transmits data in parallel form between measuring equipment or instruments and a PC, allowing the user to set up automised test routines.

Serial busses find their applications in longer length data transmission systems compared to parallel bus structures. The most widely used, and known , serial data transmision standard is the RS-232. Although originally developed for modem to terminal equipment interface is widely used as an interface for nearly all PC peripherals. For longer line lengths and better noise immunity the serial busses RS-422 and RS-485 are preferred. The bidirectional RS-485 is a popular standard becoming extensively used - especially, because of its close links to SCSI.

At the longest line length level are Local Area Networks (LAN), like Token Ring and Ethernet. TI has recently introduced a transceiver function to address the requirement of the Ethernet repeater function.

Home Automation is a growing area for future data communication. A standard like CEBus (Consumer Electronics Bus) is an example of a bus structure including more than just the electrical specification . The specification includes a robust protocol for interconnecting consumer appliances to form an intelligent network opening up a world of new possibilities in the home.

In support of the mentioned bus structure standards, Texas Instruments offers the industry's most comprehensive line of bus products, from off-the-shelf product line support to complete chip-set solutions.

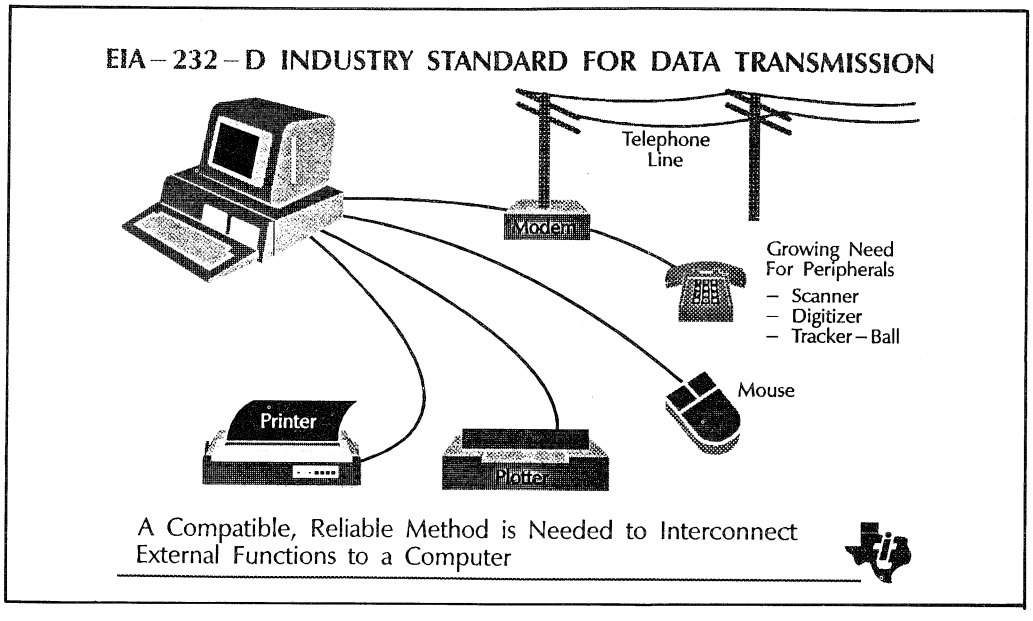


Figure 1-EIA-232-D INDUSTRY STANDARD FOR DATA TRANSMISSION

The Electronic Industries Association (EIA) introduced the RS232 standard in 1962 for the purpose of standardizing the interface between Data Terminal Equipment (DTE) and Data Communication Equipment (DCE).

Although emphasis was then, and still is, on interfacing between a modem unit and a data terminal equipment, this standard is also applicable to serial binary interfacing between various types of data terminal equipment.

The application areas for the standard have been extensively increased with the wide use of PCs, where RS232 has been adopted as the interface to peripherals such as the mouse, plotter, scanner, digitizer, printer and tracker-ball in addition to the modem unit.

Using a common standard allows widespread compatibility plus a reliable method for interconnecting a PC to peripheral functions.

The revised standard of 1969, EIA RS-232-C has now been superceeded by EIA-232-D (1986) which brings it in-line with CCITT V24, V28 and ISO IS2110. The latest revision

reflects the addition of mechanical specifications for the interface connector, loopback and test modes as the major changes.

Although an "old" standard with problems like high noise susceptibility, low data rates and very limited transmission length, RS232 provides a low cost communication solution and new products are being developed with a rate faster than ever.

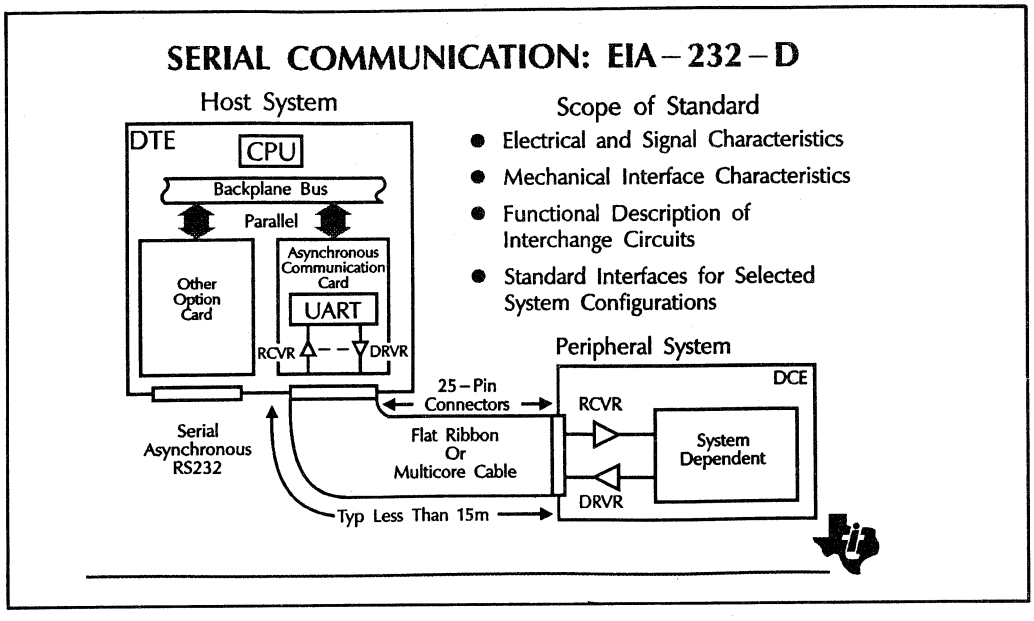


Figure 2 - EIA-232-D: SERIAL COMMUNICATION

Scope of Standard:

- O Electrical and Signal Characteristics of the interchange signals and associated circuitry in terms of signal levels, impedances and rates of change.

- O Mechanical Interface Characteristics defined as a 25 way "D" connector, with dimensions and pin assignments specified in the standard. Although the standard only specify a 25 pin D type connector, most laptop PCs today use a 9 pin "DB9S" connector.

- O Functional Description of the Interchange Circuit which enables a fully interlocked handshake exchange of data between equipments at opposite ends of a communication channel. However, V24 defines many more signal functions than RS232, but those that are common are compatible. 22 of the 25 connector pins have designated functions, although few, if any, practical implementations use all of them. The most common used signals are:

- SIGNAL GROUND (7) - interface ground reference

- TRANSMITTED DATA (2) from the DTE to the DCE. Data must be transmitted only when REQUEST TO SEND, CLEAR TO SEND, DCE READY, and DTE READY are all in the 'ON' state (positive interchange voltage). A common reason why "standard" RS232 devices fail to work together is that one implements only some of these four handshake signals, but the other is expecting them all.

- RECEIVED DATA (3) from the DCE to the DTE.

- REQUEST TO SEND (4) - the DTE telling the DCE it wants to transmit. Also used to control direction of communication in half duplex system.

- CLEAR TO SEND (5) - the DCE telling the DTE, in response to REQUEST TO SEND and its own ready condition, that the DTE may transmit.

- DCE READY (6) - the DCE telling the DTE that it is connected to a communications channel and all dialling, talking, testing etc is over. (Also called Data Set Ready.)

- DTE READY (20) - the DTE telling the DCE that it is ready to transmit or receive data.

- RECEIVED LINE SIGNAL DETECTOR (8) - the DCE telling the DTE that it is receiving valid signals over the channel. Sometimes called Carrier Detect.

- RING INDICATOR (22) - the DCE telling the DTE that a ringing signal is being received on the communication channel. (Used in auto-answer systems.)

O Standard Interfaces for Selected System Configuration outlining the use of interchange signals for different applications.

Note, that RS232 is not a standard for interface between computers and printers, although it often is used as such. Also, RS232 is not only an asynchronous communication standard. In fact it contains provisions for synchronous communication if desired. RS232 does not specify a communication format. The good old "one start bit, eight data bits and two stop bits" is not a part of the standard, although it is the most common application. Finally, RS232 is a single ended transmission standard where only one receiver is connected to each driver. developed devices (LT1080 and LT1081 from Texas Instruments) with tri-state driver and receiver outputs allow for multiple access to a single line, but there is no provisions for local area network in the RS232 standard.

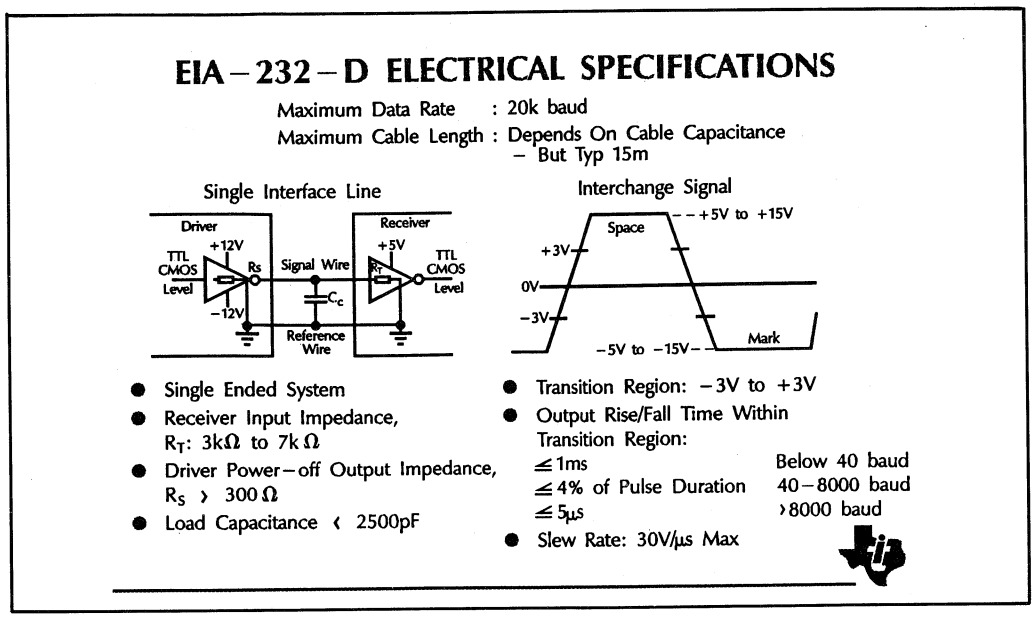


Figure 3 - EIA-232-D: ELECTRICAL SPECIFICATIONS

Data transmission using RS232 is relatively slow. The RS232 standard specifies a nominal upper limit for the data signalling rate of 20,000 bits per second (20kbaud). Transmission line effect at such data rates and short line lengths can be ignored, hence load resistance and capacitance can be regarded as lumped parameters.

Some applications use however data rates well beyond the maximum 20kbaud but faster transmission standards like RS423, RS422 and RS485 must be recommended.

The cable length is in RS232C specified to maximum 15meters but is not mentioned in EIA-232-D, as the maximum length is normally limited by the load capacitance from the cable (typ 150pF/m). The EIA-232-D specify a maximum generator or driver load capacitance of 2500pF. The combination of the driver's output current capability, the load capacitance (cable length) and the standard's switching requirements should be considered in every design, especially if CCITT V28 should be met, but are often ignored.

RS232 is a single ended transmission system making the transmission susceptible to noise and common mode signals.

A driver converting a TTL/CMOS signal to RS232 levels is usually supplied from +/-12V. A receiver converting RS232 levels to TTL/CMOS levels requires only a single +5V supply. The receiver input impedance, specified to be in the range from 3k to 7k(ohm), combined with the signal levels dissipate considerable power - even if no transmission takes place.

A receiver treats a signal above +3V as a logic zero, a "space" or an "ON" condition. A between -3V and +3V is the transition region. The generator or driver must provide a minimum of +5V and a maximum of -5V at the interface point (any point between driver and receiver).

A minimum time for the signal to stay in the transition region is specified depending of the data rate in order to reduce susceptibility to noise during transition and maintain a well defined signal for asynchronous applications. Also, a maximum dv/dc of 30V/µs minimizes cable crosstalk, high frequency switching emmission and interference with other signals.

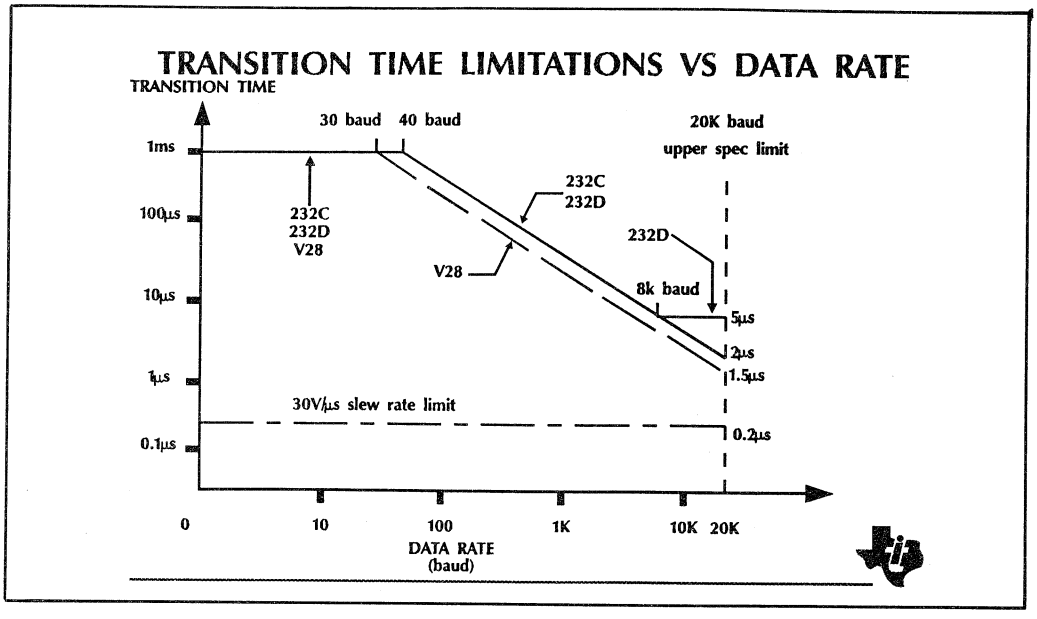


Figure 4 - TRANSITION TIME LIMITATIONS VS DATA RATE

The time required for data and timing signals to pass through the -3V to +3V transition region is shown in graphic form versus data rate for the standards: EIA RS-232-C, EIA-232-D and CCITT V28. The 30V/µs maximum slew-rate and the upper data rate of 20kbaud limit are also added, restricting the signal transition to a well defined area. The transition time for control signals should not exceed 1ms.

Note that the requirements of the CCITT specification V28 are stricter than either revisions of "232". V28 states that "the time required for a signal to pass through the transition region during a change should not exceed 1ms or 3% of the nominal element period on the interchange circuit, whichever is less". RS-232-C allows the transition time to be 4% of the duration of a signal element. EIA-232-D represents a relaxation at data rates above 8k baud where the maximum transition time becomes flat at 5µs. This means that all devices meeting V28 and RS-232-C will also meet EIA-232-D.

The practical implications of these limitations, of the driver's maximum output current, are related to the maximum cable length at a given data rate.

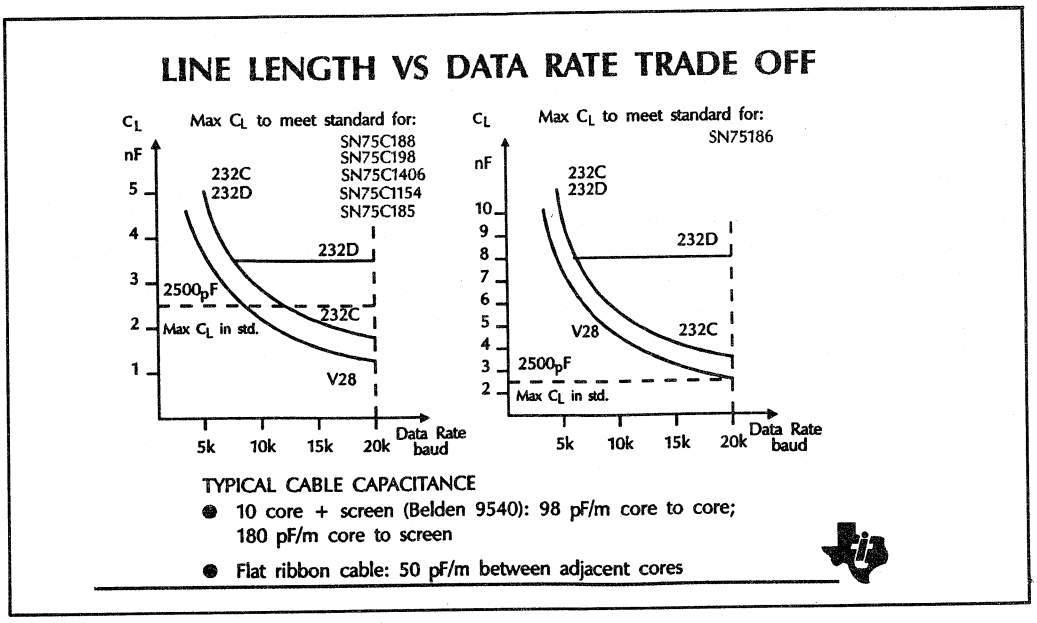


Figure 4A - THE LINE LENGTH vs. DATA RATE TRADE OFF

By taking the transition time limitations from the different standards, as shown on the previous slide, and combining them with the guaranteed driver output current capability of a driver loaded with various capacitance values, the illustrated graphs were obtained.

The equation used was derived from the transition time, t_T :

$$t_T = R_i \; C_L \; \ln\left(\frac{|R_i \; I_o \;| + |\; V_F|}{|R_i \; I_o \;| - |\; V_I|}\right)$$

where
R_i = Minimum input impedance of the receiver = 3k Ω
C_L = Load capacitance, mainly cable capacitance
I_o = Guaranteed minimum current the driver can source or sink
V_F = Final voltage = +3V
V_I = Initial voltage = -3V

Solving the equation with respect to C_L gives,

$$C_L = t_T \; / \; Ri \; \ln\left(\frac{|R_i \; I_o \;| + |\; V_F|}{|R_i \; I_o \;| - |\; V_I|}\right) = t_T \; / \; 3_T \ln\left(\frac{3\,|\,Io| + 3}{3\,|\,Io| - 3}\right) \text{ nF} \qquad \begin{matrix} t_T \text{ in } \mu s \\ I_o \text{ in mA} \end{matrix}$$

Note that t is a function of the data rate and standard as shown on the previous slide. I_o varies from device type to device type.

The maximum load capacitance to meet the standards in terms of transition time is shown on the graph to the left. All devices are based on similar silicon cells. The conclusion is, that they can all drive in excess of 3500pF (corresponding to a typical cable length of 20m with

180pF/m) to 20kbaud and still meet EIA-232-D. However, if CCITT V28 must be met, the data rate is restricted to less than 10kbaud with the maximum specified cable load capacitance of 2500pF. If the data rate has to be 20kbaud then the cable length should be less than 6m (using a typical cable capacitance of 180pF/m).

A similar graph is drawn to the right, for another new device SN75186 featuring a very high output drive capability. Note the changed scale on the C_L axis. This device has been particularly designed to meet the CCITT V28 specification at the maximum specified data rate and cable load capacitance. This device is of course well suited for applications using line lengths or data rates beyond the standards. SN75186 can drive 45m cable (using a typical cable capacitance of 180pF/m) to 20kbaud and still meet the transition time requirements of EIA-232-D!!

All of the above calculations are based on worst case conditions. Typical specifications would yield far better drive capability.

At high transmission speeds beyond the specifications of the standard, the data rate is not only limited by the transition time but also by the delay of the built-in receiver filter.

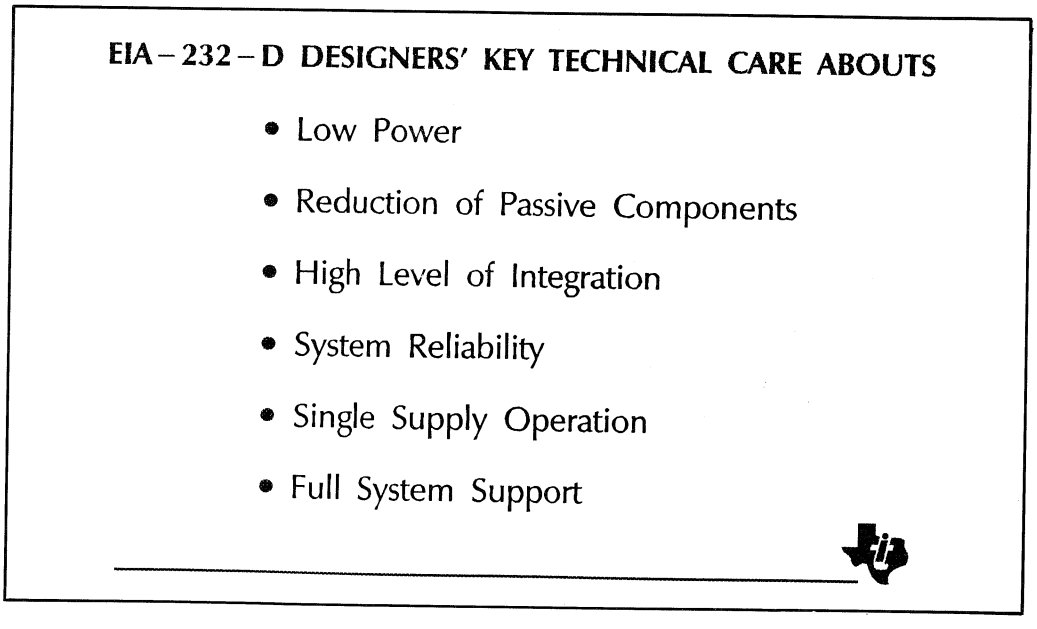


Figure 5 - EIA-232-D: DESIGNER'S KEY TECHNICAL CARE ABOUTS

The increasing use of laptop PCs and portable equipment with RS232 interface, demands low power devices. Also the increasing integration of modems, PCs and their peripherals requires elimination of passive components and single chip RS232 solutions.

In systems like host terminal controllers where many RS232 devices are used, system down time is expensive and high reliability and self-test capability is required for faster fault diagnosis.

In computers with disk drives dual supplies are usually available, but many industrial and modem applications need RS232 devices capable of operating from a single +5V supply.

Most RS232 systems use asynchronous data transfer and require a communication controller for the parallel to serial data conversion and visa versa. Other systems utilize a serial port on the microprocessor.

Texas Instruments provides the complete RS232 solutions including popular UARTS.

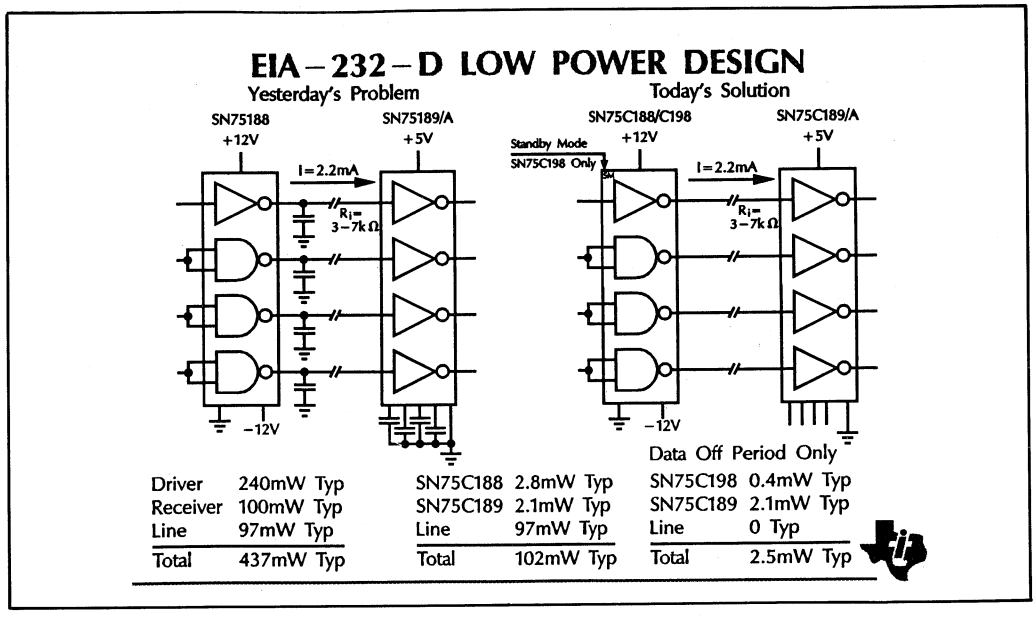


Figure 6 - EIA-232-D: LOW POWER DESIGN

Most devices used today like the MC1488/SN75188 and MC1489/SN75189 are fairly old designs using a lot of power. New developments like the SN75C188 and SN75C189 have yielded low power devices offering insignificant quiescent power consumption compared with the line current. (Line current flows from the driver output through the receiver input impedance: typically 5kΩ as specified by the standard). This current flows even when no data are transmitted.

One way to reduce this line current in data off periods is to employ a driver with tri-state output feature like the SN75C198. By disabling the output the power consumption can be reduced to less than 1% of the old SN75188/SN75189 system.

SN75C188, SN75C198, SN75C189 and SN75C189A are designed in a low power robust BIPOLAR/BIMOS process. The power saving when compared to industry standard devices is shown below;

Driver	240	mW	Typ	SN75C188	2.8	mW	Typ	SN75C198	0.4	mW	Typ
Receiver	100	mW	Typ	SN75C189	2.1	mW	Typ	SN7C189	2.1	mW	Typ
Line	97	mW	Typ	Line	97	mW	Typ	Line	0	mW	Typ
Total	437	mW	Typ	Total	102	mW	Typ	Total	2.5	mW	Typ

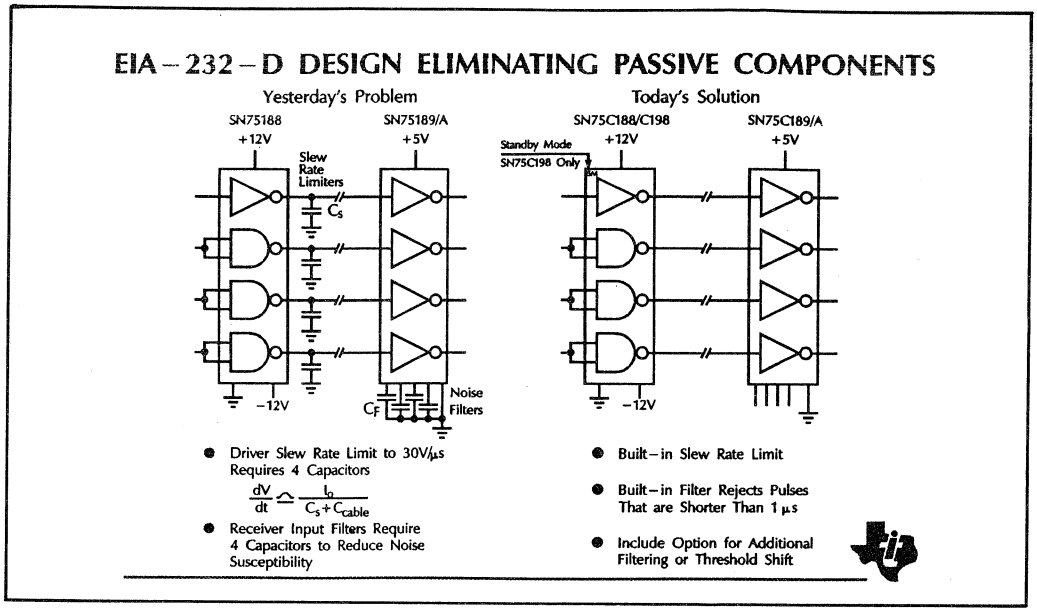


Figure 7 - EIA-232-D: DESIGN ELIMINATING PASSIVE COMPONENTS

The most widely used devices require capacitor bypassing to ground of all the lines to reduce the maximum slew-rate of 30V/μs specified by the standard. The capacitor value, C_S can roughly be estimated from the maximum driver output current and the cable capacitance. The cable length and capacitance is usually not a fixed parameters. However with a maximum output current of 12mA from SN75188 a 400pF capacitor for C_S will ensure operation within the standard even without a loading cable.

When communicating between the elements of a data processing system in a hostile environment, spurious data caused by, ground shifts and noise signals may be introduced, therefore it can become difficult to distingquish between a valid data signal and those introduced by the environment. To overcome this problem in systems using older devices, a RC receive filter is formed by a part of the receiver's resistive input impedance and an external capacitor, C_F giving a single pole roll-off. This adds up to a total of 8 capacitors required per quad driver and receiver pair for proper operation.

The new SN75C188, SN75C198, SN75C189 and SN75C189A designs feature built-in slew-rate limitation that meets the standard under all load conditions. Furthermore a unique built-in receive filter rejects all signals below 1μs of duration, regardless of voltage amplitude, and accepts all signals longer than 4μs as valid data.

Obviously, the new designs eliminate 8 external passives per driver/receiver pair.

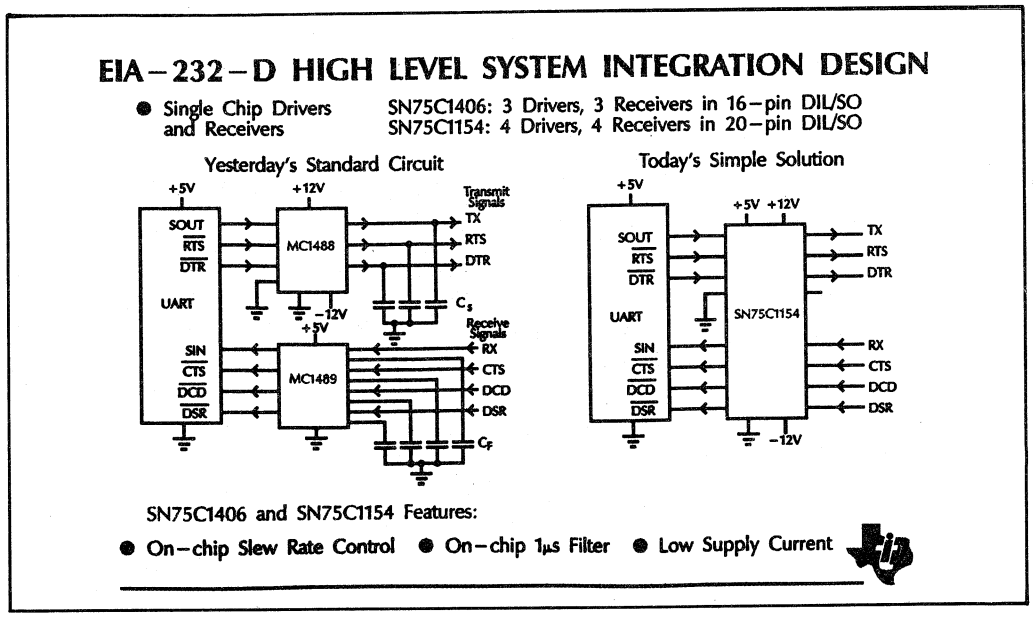


Figure 8 - EIA-232-D: HIGH LEVEL OF SYSTEM INTEGRATION DESIGN

For systems requiring 3 driver/receiver pair and less or 4 driver/receiver pair and less, SN75C1406 or SN75C1154 are highly integrated single chip solutions. The devices are based on the same cells as SN75C188 and SN75C189 and hence offer the same features and associated benefits.

In this application only a few handshake lines are used in addition to the data lines. A transmission from the DTE (this device) to the DCE is initiated from the DTE by issuing a RTS (Request to Send). The DCE respond to this signal with a CTS (Clear to Send). The DCE tells the DTE that dialing is completed and that the communication channel is connected by issuing a DSR (Data Set Ready or DCE Ready). The DTE tells the DCE that it is ready to transmit data by issuing a DTR (DTE Ready) signal. When all these four handshake lines are in the "ON" state, data must be transmitted.

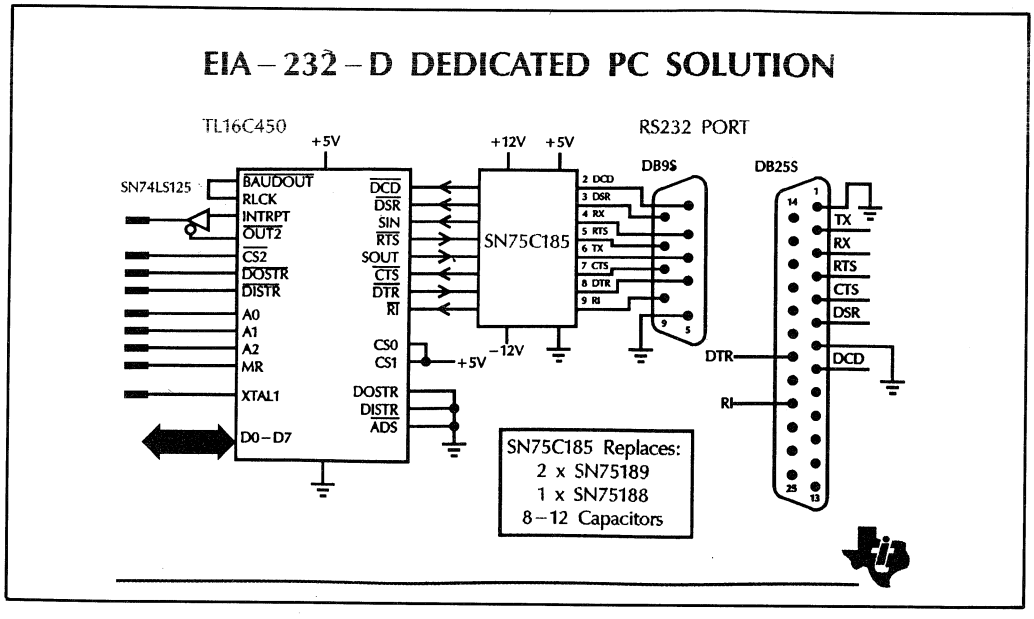


Figure 9 - EIA-232-D: DEDICATED PC SOLUTION

IBM compatible PCs use three drivers and five receivers for their RS232 ports. The SN75C185 (based on the SN75C188 and SN75C189 cells) has been optimised for this particular application replacing the two SN75189 and one SN75189 previously required, plus eliminating the associated capacitors.

The SN75C185 pinout has been optimised to line up with the 9 pin DB9S connector used in laptop PCs for which the low power consumption of the SN75C185 is ideally suited. This highly integrated driver/receiver with on chip driver slew-rate limiter and receive filter, together with the TL16C450 UART forms a simple solution to a single RS232 port.

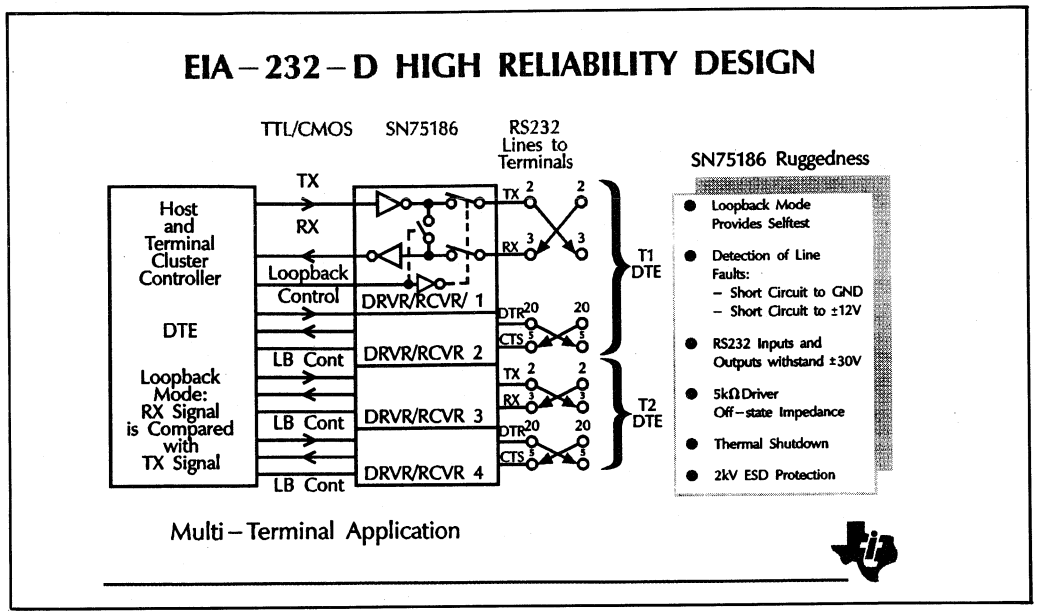


Figure 10 - EIA-232-D: HIGH RELIABILITY DESIGN

In systems where a central host communicates with several terminals a large number of RS232 devices are used. System failures can be difficult to identify and host down time is expensive. Sitting closest to the outside world makes the RS232 devices most vulnarable to failure, often caused by excessive external signals being applied to the transmission line.

The major consideration for RS232 devices in such applications are robustness and the ability to test themselves under software control from the host (without the need for disconnecting cables and manually inserting a loopback connector.) Such a feature could facilitate faster fault diagnosis and significantly reduce equipment down time.

These requirement has driven the need for the SN75186, an extremely robust quad driver and receiver with loopback selftest capability. The device includes the usual on chip driver slew-rate control and receiver filter. In addition, this device features a high minimum short circuit output current allowing it to fully comply with the CCITT V28 transition time requirements at full capacitive load and maximum data rate. This drive capability is unique in the market.

The device's robustness is borne out by an ESD rating of 2kV, a rating which can not be met by standard devices in the market, and the ability to withstand +/-30V at any RS232 input or output whilst powered or unpowered. Its loopback feature allows software controlled testing of nearly 100% of the device's circuitry as well as short circuit to ground or either supply rails. Loopback testing of a single driver/receiver pair is initiated by activating its loopback control pin. This disconnects the RS232 line and feeds the driver output back through the receiver input for comparison within the host to determine if the functional operation of the driver and receiver together is correct.

Flexibility of this control is ensured by each driver/receiver having its own loopback control input. In the case of a permanent output short or other problems resulting in a very high

chip temperature, a thermal shutdown facility protects the device against damage. During this thermal shutdown mode the output goes into a high impedance state and the receiver is held in a logic high (marking) state.

The application shown details the interface between a single SN75186, the host and two connected terminals - both host and terminals operate as DTEs. A very simple host to terminal interface is employed using only two handshake lines: CTS and DTR in a cross connection.

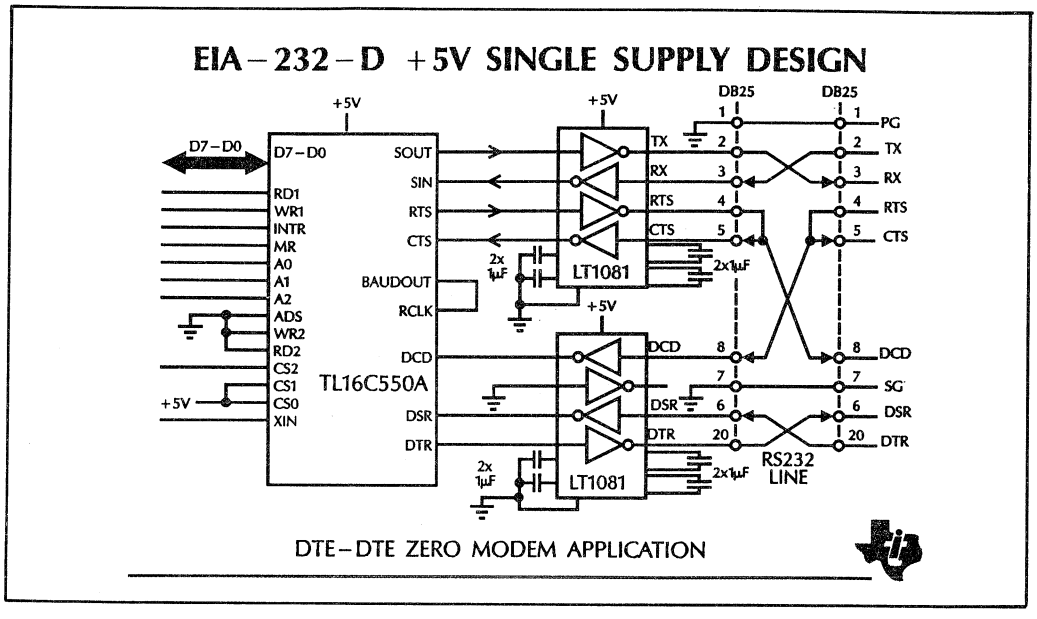


Figure 11 - EIA-232-D: +5V SINGLE SUPPLY DESIGN

In pure digital systems where no +/-12V supplies are available for, a key requirement is for a device capable of operating from a single +5V supply. This can be achieved by RS232 devices with internal chargepump to step-up and invert a +5V supply voltage to +/-9V supplies to ensure that the minimum +/-5V voltage swing on the RS232 line can be acheived.

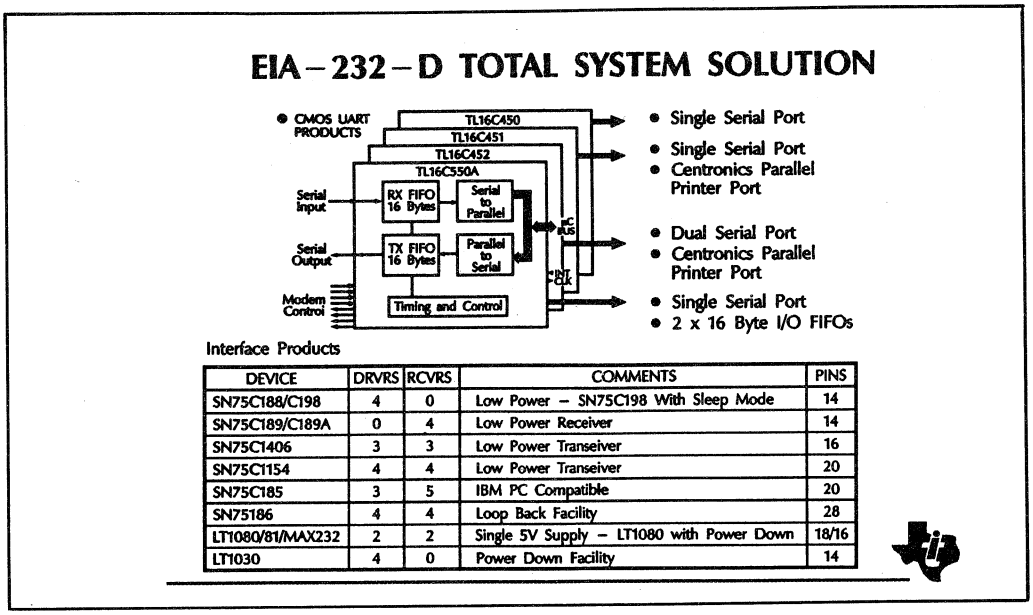
LT1080 and LT1081 are devices available from Texas Instruments featuring an internal chargepump facillitating single supply operation. Two 1µF capacitors are required for the charge pump operation and two additional 1µF capacitors are used for smoothing of the generated dual voltages. The chargepump provides enough current for driving low power external circuitry such as other RS232 drivers or op amps. However, they should be loaded with care, since excessive loading can cause the generated supply voltages to drop, causing the RS232 driver output voltages to fall below RS232 requirements.

The LT1080 features a shutdown mode, that in addition to a power reduction puts both the driver and receiver outputs in high impedance states, thus allowing for several devices to share a receiver and driver line. Also a transceiver configuration is possible. However, the EIA-232-D makes no provisions for such operation.

In this particular application the LT1080 is a DTE to DTE communication link (also called a "zero or null modem" application.) All data and handshake lines are cross coupled.

The UART (TL16C550A) has 16 bytes receiver and transmitter FIFOs which reduces the number of interrupts to the microprocessor.

For more cost sensitive applications the MAX232 is also available form Texas Instruments. The MAX232 is functionally the same as the LT1080/81 and has the same pin out as the LT1081.



DEVICE	DRVRS	RCVRS	COMMENTS	PINS
SN75C188/C198	4	0	Low Power – SN75C198 With Sleep Mode	14
SN75C189/C189A	0	4	Low Power Receiver	14
SN75C1406	3	3	Low Power Transeiver	16
SN75C1154	4	4	Low Power Transeiver	20
SN75C185	3	5	IBM PC Compatible	20
SN75186	4	4	Loop Back Facility	28
LT1080/81/MAX232	2	2	Single 5V Supply – LT1080 with Power Down	18/16
LT1030	4	0	Power Down Facility	14

Figure 12 - EIA-232-D: TOTAL SYSTEM SOLUTION

Most RS232 systems use industry standard UARTS. The TL16C450 is the basic part for PC's as well as other applications. Features include:

- Programmable baud rate generator
- Adds and deletes standard asynchronous communication bit
- Fully programmable serial interface characteristics
- Data communication diagnostic capability
- Modem control functions
- Simple interface to microprocessors
- Maximum data rate of 256kbaud

The TL16C451 is similar to TL16C450 with the single serial port with the addition of a Centronic parallel printer port. The IBM PC AT/XT sets the standard for this parallel printer interface which all "compatible" manufactures have to follow. TTL-level signals are presented on a 25 pin D-type socket. Apart from the choice of connector it is directly compatible with the "Centronics" standard printer interface.

The TL16C452 has two serial ports plus a parallel Centronics printer port. Using this UART together with two SN75C185 provides a simple 3 chip complete solution for the two RS232 ports plus a printer port which is common on basic PC configurations.

The TL16C550A is similar to the TL16C450, but two 16 bytes FIFOs buffer the transceiver and receiver data stream further reducing the number of interrupts from the microprocessor.

The range of RS232 drivers and receivers shown are the latest additions to Texas Instruments range of industry standard devices.

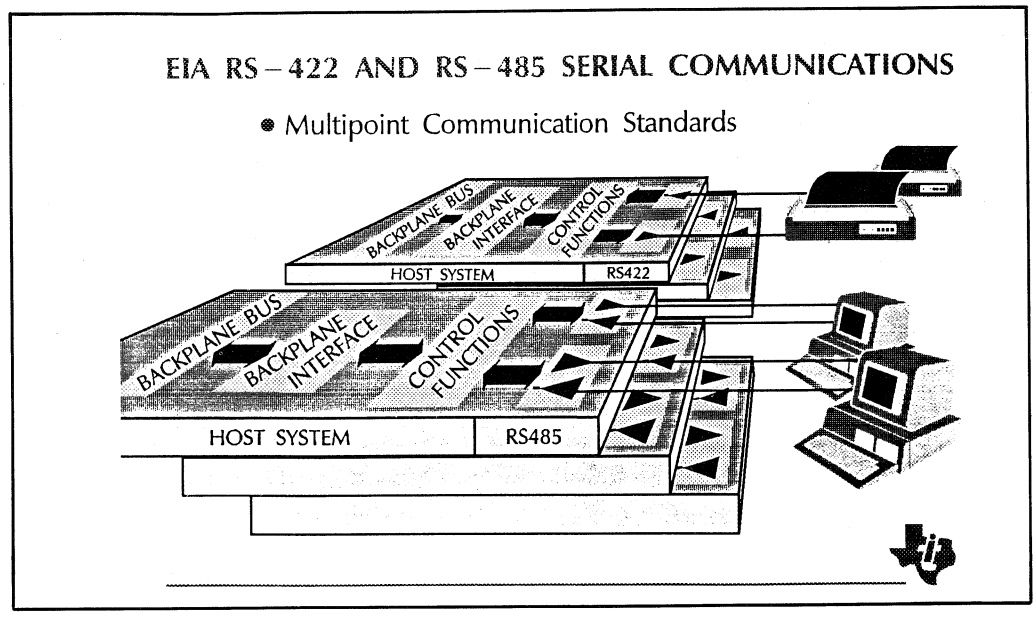


Figure 1 - EIA RS-422 and RS-485 Serial Communications

High speed data transmission between computer system components and peripherals over long distances, under high noise conditions, usually proves to be very difficult if not impossible with single-ended drivers and receivers. Recommended EIA standards for balanced digital voltage interfacing provide the design engineer with a universal solution for long line system requirements.

RS-422 and RS-485 are balanced (differential) digital transmission line interfaces developed to incorporate and improve upon the advantages of the current-loop interface and improve on the RS-232 limitations such as:

- Data rate (up to 10M baud)
- Longer line length (up to 1200 meters)
- Differential transmission (less noise sensitive)

RS-422 offers a reliable multipoint one way communication. A typical application area is its use in transmitting data from a central computer to multiple remote monitors, printers or stations, such as airport arrival and departure monitors.

RS-485 is an upgraded version of RS-422 extending the number of peripherals and terminals that a computer can interface to. Additionally, RS-485 allows for bidirectional multipoint party line communication and can effectively be used for "mini-LAN" applications, such as data transmission between an advanced cash check-out point and a central computer in a supermarket.

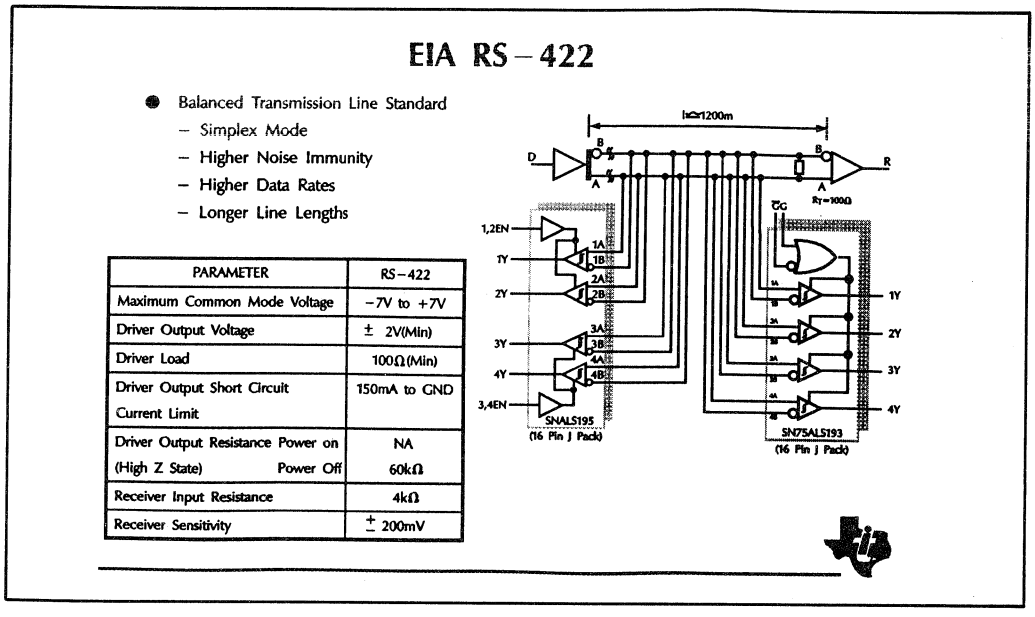


Figure 2 - EIA RS-422

EIA RS-422-A is a balanced transmission line standard developed in 1975 to interface a host computer's data, timing or control lines to its peripherals.

A RS-422 line allows for only one way communication (simplex mode) but by using a differential twisted pair transmission media (not specified in std.) and a RS-422 receiver with its min 7V common mode voltage capability makes it less susceptable to noise picked up in hostile environments via the long cables. The specification in the standard places no restrictions on minimum or maximum operating data rates but rather on the relationship of transition speeds to a unit interval. However, data rates up to 10M bit per second are supported and line lengths up to 1200 metres is given as guideline but not at maximum data rate.

When operating at low data rates (below 200k bit per second) or at any speed where the signal rise time at the drive end of the cable is greater than 10 times the one-way propagation delay time of the cable, the transmission is not particularly sensitive to the presence of a proper cable termination. Under all other conditions cable loading can no longer be considered as a lumped parameter and transmission line considerations must be applied.

The characteristic impedance of twisted pair cable is a function of frequency and cable type. Typical twisted pair cables have a 100-120 Ohm impedance. A termination resistor with an impedance similar to the cable's characteristic impedance should only be connnected at the furthest end of the cable.

SN75ALS193 and SN75ALS195 represent two quad receivers with different enable structures. Their common mode range extends from -7V to +7V maximum with maximum +/- 200mV signal sensitivity. The compatible drivers are SN75ALS192 and SN75ALS194. The ALS devices are designed to operate at data rates upto and even in excess of 10M bit per second while offering lower power compared to slower previous LS parts. Texas Instruments has a wide range of devices supporting this standard. Please consult the data book for more information.

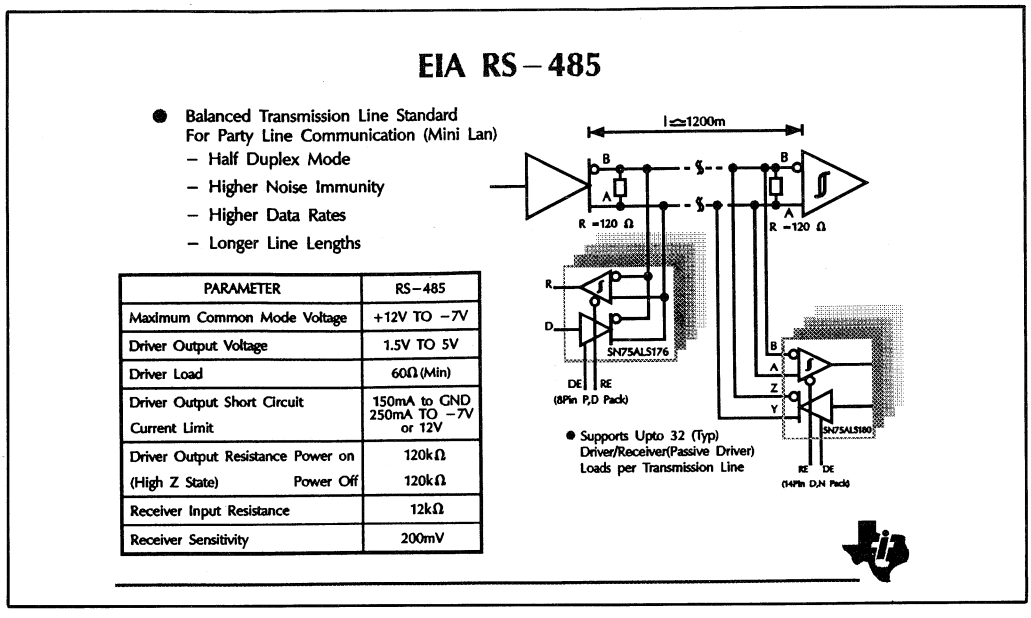


Figure 3 - EIA RS-485

EIA RS-485, introduced in 1983, is an upgraded version of EIA RS-422-A. Increasing use of balanced data transmission lines in distributing data to several system components and peripherals over relatively long lines brought about the need for multiple driver/receiver combinations on a single twisted pair line.

RS-485 takes into account RS-422 requirements for balanced-line transmission plus additional features allowing for multiple drivers and receivers. Standard RS-485 differs from the RS-422 standard primarily in the features that allow reliable multipoint communications. For the drivers these features are:

- One driver can drive as many as 32 unit loads (one unit load is typically one passive driver and one receiver).

- The driver output, off-state, leakage current shall be 100uA or less with any line voltage from -7V to +12V.

- The driver shall be capable of providing a differential output voltage of 1.5V to 5V with common-mode line voltages from -7V to 12V.

- Drivers must have self protection against contention (multiple drivers contending for the transmission line at the same time).

For receivers these features are:

0 High receiver input resistance, 12kΩ minimum.

0 A receiver input common-mode range of -7V to 12V.

0 Differential input sensitivity of +/-200mV over a common-mode range of -7V to 12V.

The guidelines for data transmission speeds, cable lengths and media are the same as for RS-422.

SN75ALS176 and SN75ALS180 are examples of transceivers and drivers/receivers available from Texas Instruments. The ALS devices feature data rates up to 23M bit per second.

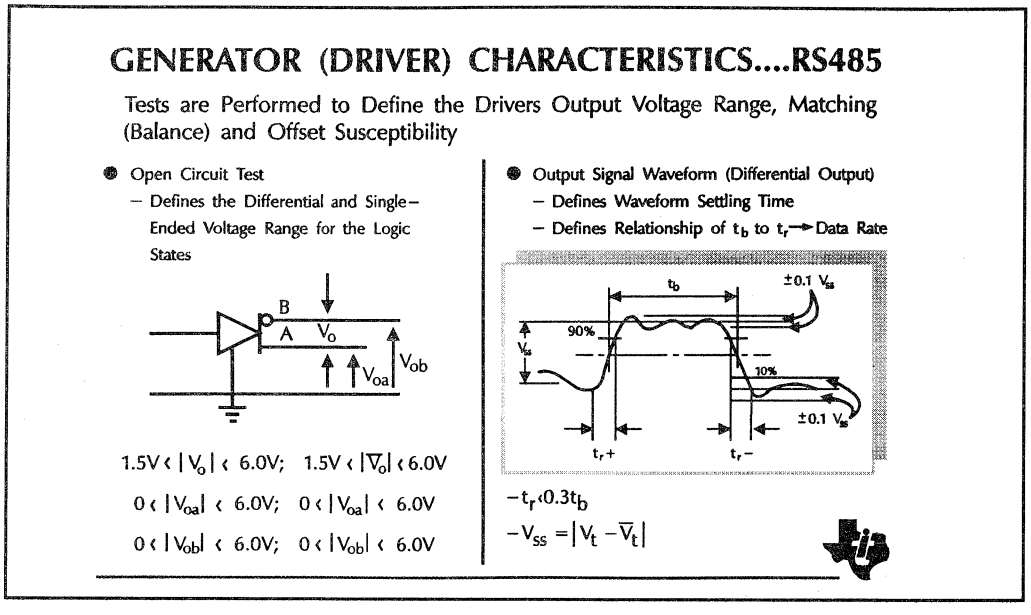


Figure 4 - Generator (Driver Characteristics).....RS-485

Open circuit test (left figure) defines the differential and single-ended voltage range for the logic states as follows:

For either logic or binary state, the magnitude of the differential voltage, Vo measured between the two driver output terminals shall be not less than 1.5V and not more than 6V; and the magnitude of Voa and Vob measured independently between each generator output terminal and generator circuit ground shall be not more than 6V.

Output signal waveform (right figure). During transition of the generator output between alternating binary states, the differential voltage measured across a test load 54 Ω in parallel with 50pF connected between the driver outputs terminals shall be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS} within less than 0.3 of the unit interval. Thereafter, the signal voltage shall not vary more than 10% of VSS (voltage between the two state values of the generator output) from steady state value, until the next binary transition occur. The instantaneous magnitude,

V_t and V_t of either binary state shall not exceed V_{SS} or 5V.

RS-485 defines the device transition time, tr relative to one unit interval, tb. If transition time for a device is known then the maximum operating data rate, fb for RS-485 conditions can

be calculated as follows:

tr = 0.3 tb or tb = tr/0.3;

For example, the SN75172 driver has a specified maximum tr of 120ns. At worst case the maximum data rate would be:

fb = 0.3/(120ns) = 2.5M bit per second.

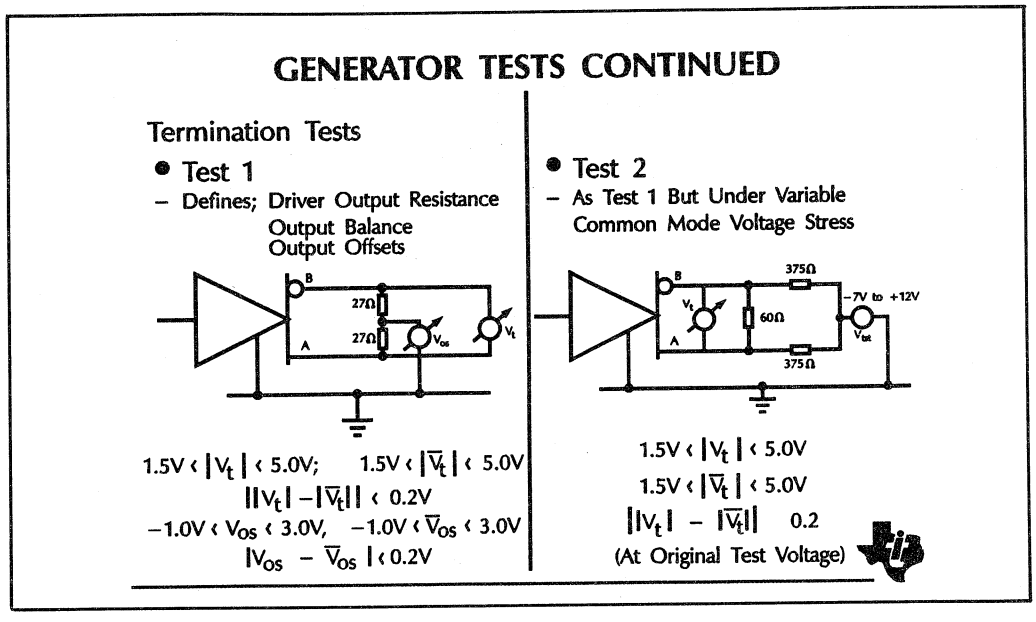


Figure 5 - Generator Tests Continued

Termination tests 1 defines output resistance, balance and offsets:

With a test load as shown, the magnitude of the differential voltages, Vt and the offset voltages, Vos should be as specified.

With a test load as shown, the magnitude of the differential voltages, Vt under worst case common-mode signal (-7V to 12V) conditions should be as specified.

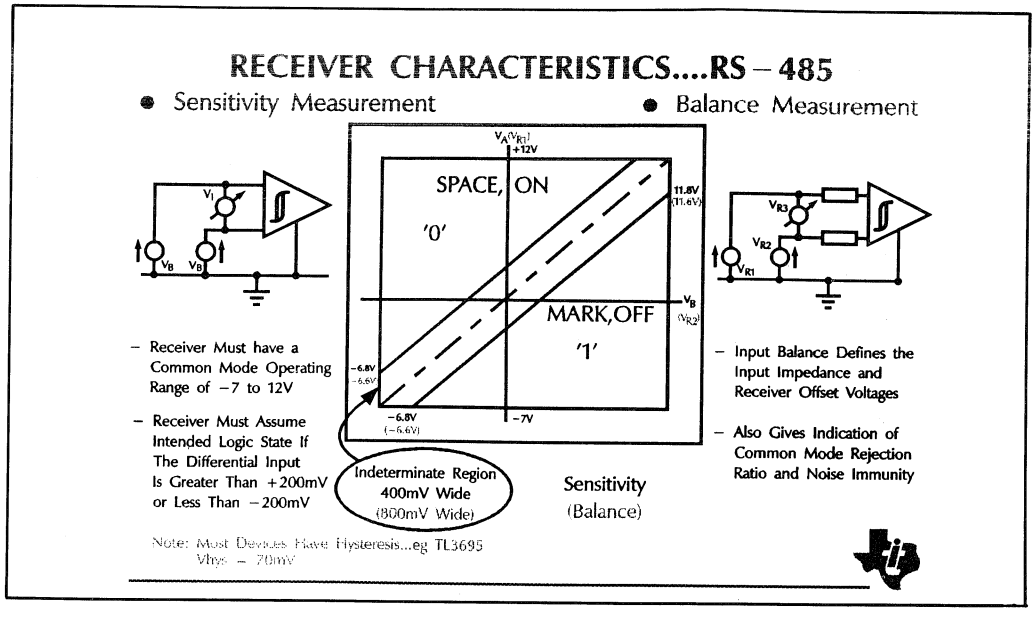


Figure 6 - Receiver Characteristics....RS-485

Sensivity measurements. The allowable range of input voltages appearing at the receiver input terminals measured with respect to receiver common shall be between -7V and 12V. For any combination of receiver input voltages within the allowable range, the receiver shall assume the intended binary state with an applied differential input voltage of +/-200mV or more. To avoid faults from noise on slow rising/falling signals, receivers have usually incorporated hysteresis like the TL3695 with Vhys = 70mV.

Input balance measurements defines the input impedance and receiver offset voltage and give indication of how well a device rejects common-mode signals.

With a test configuration as shown, a differential signal of +/-400mV is applied through two equal valued (1500 Ohm /(number of unit loads) series resistors. With this signal applied, the receiver output shall remain in the intended binary state throughout the -7V to 12V common-mode range.

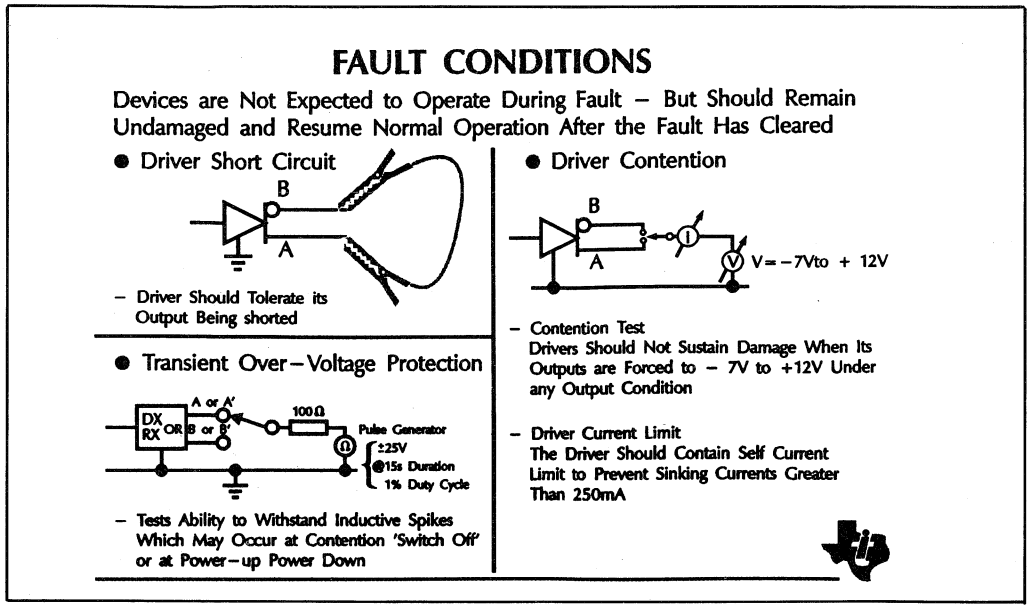


Figure 7 - Fault Conditions

RS-485 devices should not be damaged due to the fault conditions shown. On the basis of this drivers, receivers and transceivers meeting the RS-485 standard represent very reliable and robust communication products when used as specified by standard.

However, other factors in real life applications require sometimes further precaution to be taken. Excess and damaging voltage (more than +/-25V) stress on inputs can be clamped with appropriate circuitry - and excess common-mode voltage exceeding the maximum specified range (-7V to 12V) by the standard, can usually be avoided by effective grounding techniques and choice of shielded twisted pair cables as transmission media.

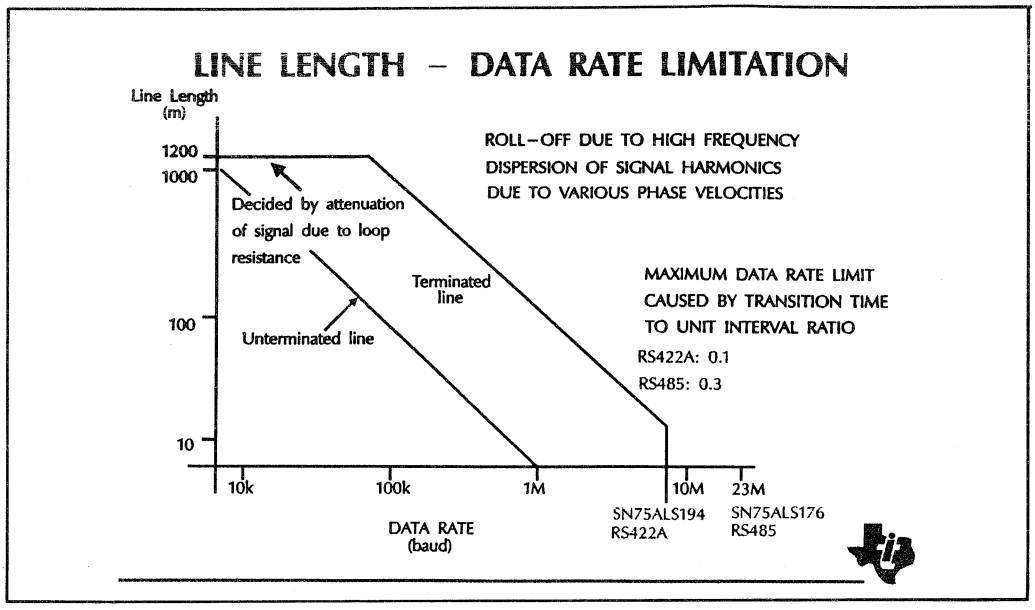


Figure 8 - Line length data rate limitation

In any system for any given application there will usually be a compromise between the line length used and the data rate required, if distortion in its many guises is to be avoided.

An important step is to look at the varrious forms of this distortion ;

No transmission line is perfect, even by just sending current down the line some voltage drop will occur due to the resistive nature of the line, this in the most simplistic form is distortion. This is compouned when longer line lengths are used where the attenuation from source to destination can cause quite severe distortion.

This places a limit on the line length even at low data rates as shown in the top left hand corner of the foil.

A typical cable of 24 SWG can have a series resistance of 80 Ω per km, and so the is limited to the order of 1200m.

Another limitation of system performance is the speed limitations of the device itself. No device has zero propagation delays and transition times. Therefore to ensure the device does not introduce distortion limits are set to define the the ratio of the unit interval ,t_b , to the signal transition times t_r.

This limitation is often specified in the standard being used. For RS-422-A the ratio of t_r to t_b is 1: 10, and for RS-485 1:3.3 . This makes it difficult to compare data rates for RS-485 and RS-422 when looking at devices compatable to both standard. The device will be specified to meet worst case conditions, that is the RS-485 specification which is tested with a 54Ω and 50p F loads and RS-422. Inspite of this the SN75ALS176 can operate at speeds upto 23 MBaud.

Other effects on the transmission line are due to phase distortion introduced on the drivers transitionional edges. The high speed edges, neccessary for high speed systems, have high frequency harmonics. The inductive and capacitive (and resistive) nature of the line introduces delay and distortion of these harmonics. This in turn reduces the clarity of the signal being sent down the line, and so increases the probability of error.

This effect is normally measured using eye patterns which measure the jitter and distortion in the signal being sent down the line. It is this effect that causes the predominant reduction in data rate as the line length increases. Another limitation can be caused by incorrect termination of the line, causing reflections. These reflections can cause errors due to loss of timing information.

In conclusion distortion and thus data interity is a function of signal rise time and line attenuation. Signal risetime and attenuation are often quoted in manufactures data, and can be used to determine the line distortion.

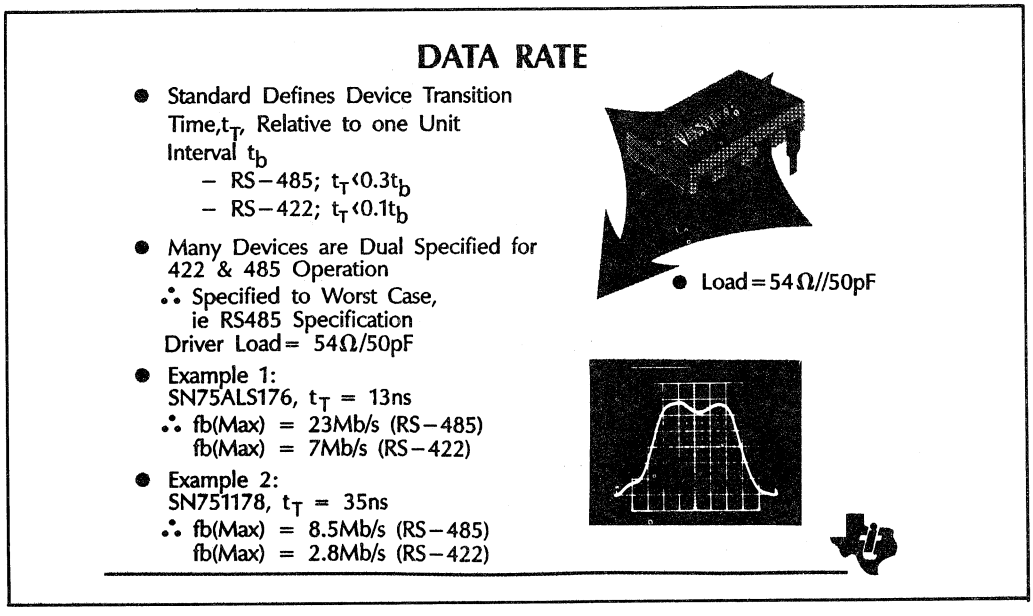


Figure 9 - Data Rate

As stated earlier there will always be a finite limit on the speed that data can be sent down a line. This is a combination of many things, technology of the device being one of them.

Another limitation on the speed will be dictated by the application itself. The RS-485 and RS-422 standards specify a limit on the maximum speed of the device based on the relationship between the drivers transition edges (rise and fall times) and the unit interval. This is an arbitary level set to ensure data integrity over a wide range of applications , often this rule can be ignored - but your application will not meet the standard.

As outlined earlier the RS-422 standard has been designed for a differential simplex system with multiple receivers. Consequently the specified resistive and capacitive loading on the drivers is not as stringent as that for the RS-485 duplex mode.

A result of this is that devices meeting RS-422 normally have their transition times limited to one tenth of the smallest unit interval being used. In other words the maximum data rate is equal to ten times the reciprocal of the transition time, which is normally specified at a resistive and capacitive loading of 100Ω and 15pF respectively.

While for RS-485 the transition time is limted to three tenths of the smallest interval being used, so the maximum data rate for RS485 is equal to ten thirds of the reciprocal of the transition time. This is normally measured with a resistive and capacitive loading of 54Ω and 50pF respectively.

A high performance transceiver such as the SN75ALS176 an drive data down the line at data rates upto 23Mb/s, making it more than suitable for RS-485 and emerging systems such as SCSI. Using the same transition edge speeds for analysis on RS-422 it would seem that the 'ALS176 could drive RS-422 at only 7Mb/s, but since the device is designed for both RS-485 and RS-422 systems it had to be specified to the tighter limits.

The SN751178 designed in LS technology is a dual differential driver receiver which is capable of delivering data rates of 8.5 Mb/s for RS-485 applications and 2,8 Mb/s for RS-422. Both data rates are within the scope of the standard.

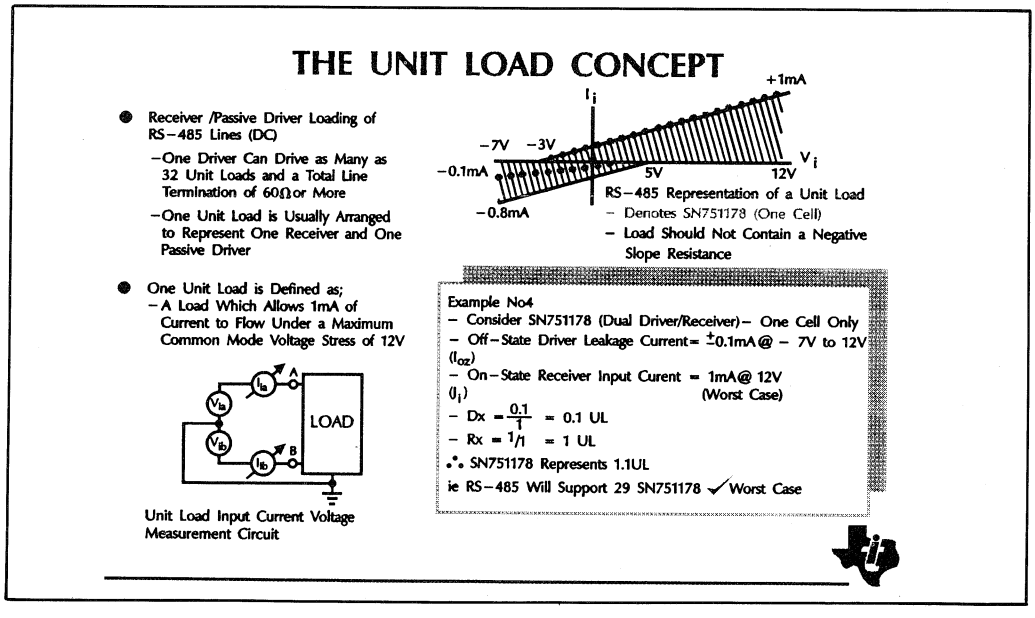


Figure 10 - The Unit Load Concept

The maximum number of drivers and receivers that can be placed on a single communication bus depends upon their loading characteristics relative to the definition of a unit load (U.L). RS-485 recommends a maximum of 32 unit loads per line.

One U.L (at worst case) is defined as aload that allows 1 mA of current under a maximum common-mode voltage stress of 12 V . The loads may consist of drivers and or receivers but does not include the termination resistors, which may present additional loads as low as 60 Ω total.

The foil shows an example of a unit load calculation, where the dual SN751178 driver receiver offers a unit load value of 1.1 U.L meaning 29 such devices could be connected on one line.

The graph in the top right is used to define the boundries of the unit load, and works by superimposing the voltage and current characteristics of the load upon a reference trace. A line from - 3 V is drawn at a tangent to intercept receiver input current at the 12 V point. Similarly a line is drawn from -7 to intercept the driver leakage current at the 5 V point. The currents indicated at - 7 V and -12 V are then compared to the ideal currents, The larger of the two ratios forms the unit load value.

The electrical characteristics should not show any negative resistance otherwise instability and spurious oscilation could occur.

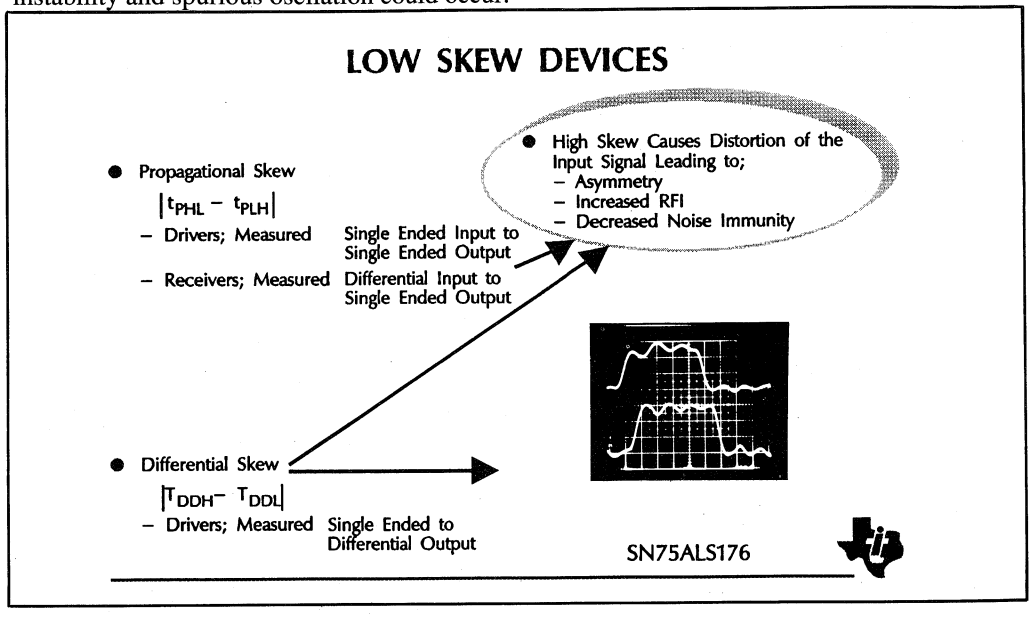


Figure 11- Low Skew Devices

When driving the line at high speeds the effects of the driver and receiver on the system become more apparent. The size of the delays relative to the unit interval increase meaning that asymmetries in the edges cause extra distortion on the output to the line.

Using differential line systems the delays through the driver and receiver have different meanings. This is because the driver is really a single ended input to differential output converter, while the receiver is a differential input to single ended converter.

When discussing propagation delays through the driver, two possibilities arise; the propagation delay from the input to one output and the other output (single ended) and also the propagation delay from the input to the differential output (differential).

The single ended propagation delay is normally measured between the input going through 1.5V and the output going through 1.5V, while the differential propagation delay is measured from the input going through 1.5V and the differential output going through its

mid-voltage, (in a balanced line 0V across the line).

These propagation delays effectively displace the signal on the line in time, but do not ideally distort it. The differences in the delays from output A going high and output B going low to output A going low and output B going high does cause distortion. The differences between these are termed as the skew in the output. For a single ended measurement it is termed the ***Propagation Skew***, while for the differential measurement it is termed ***Differential Skew***.

The main effects of propagation skew are that the differential transition edges can be stretched out and that they can become flat around the threshold region of the receiver, ie at the common mode voltage of the line. This gives the system a lower noise immunity and can increase the radiated RFI and sensitivity.

The main effect of the differential skew is the asymmetry caused by different differential propagation delays causing one state to be longer than the other state.

The propagation skew is specified on the older differential line drivers while differential skew is specifed on the more modern devices such as T.I.'s SN75ALS176.

The receivers are tested on the propagation skew. With one input tied at a reference voltage and the other toggled, giving a single ended propagation delay. The skew in this delay will also cause extra distortion to signal especially its timing information as the periods can be further distorted.

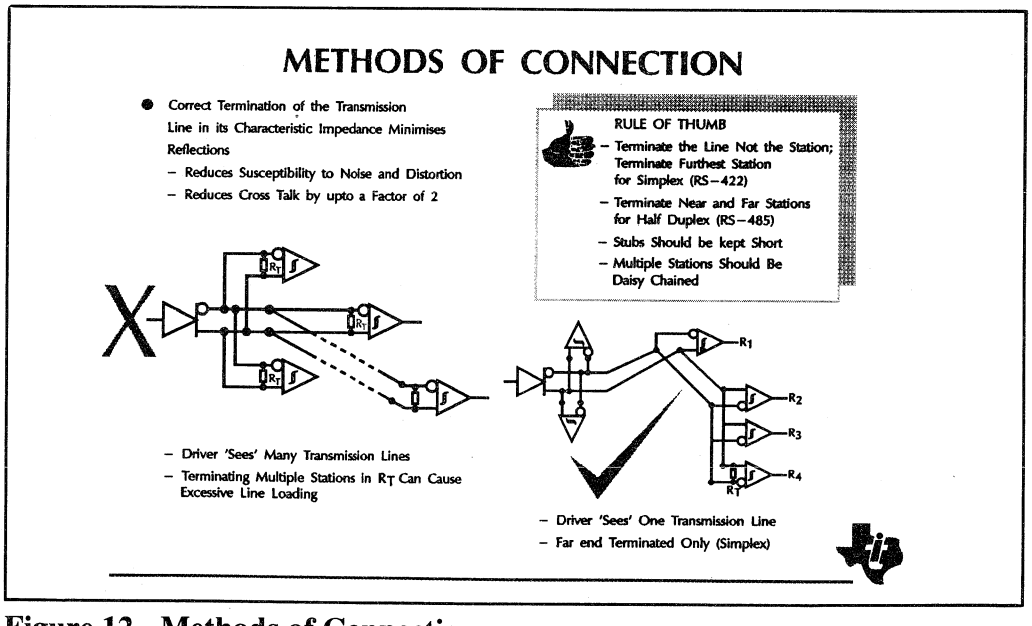


Figure 12 - Methods of Connection

Once considered as a transmission line, methods of line termination and device positioning must be considered. In particular special consideration must be given if receivers are bunched together at one end of the line. There are two basic methods of connection;

i) The star connection
ii) The daisy chain connection

Considering the star connection the transitional edge from the driver will be loaded by a group of seperate transmission lines, rather than one. Each transmission line bounary will cause a change in impedance resulting in reflections.

Another situation to avoid is the termination of multiple stations, since this could excessively load the driver. Termination at the extreme ends for RS-485 (half duplex) and far end only for RS-422 is recommended. Normally stubs (taps of the main line) should be kept as short as possible to not appear as transmission lines

The recommended method is to use the daisy chain configuration were the last receiver on the chain is terminated. This means that the transmission line and hence the driver will only see one continuing transmission line with only one termination resistor. Each tap-off will in effect be a stub but in this case they will not be all grouped together and will be quite short hence reducing their effect.

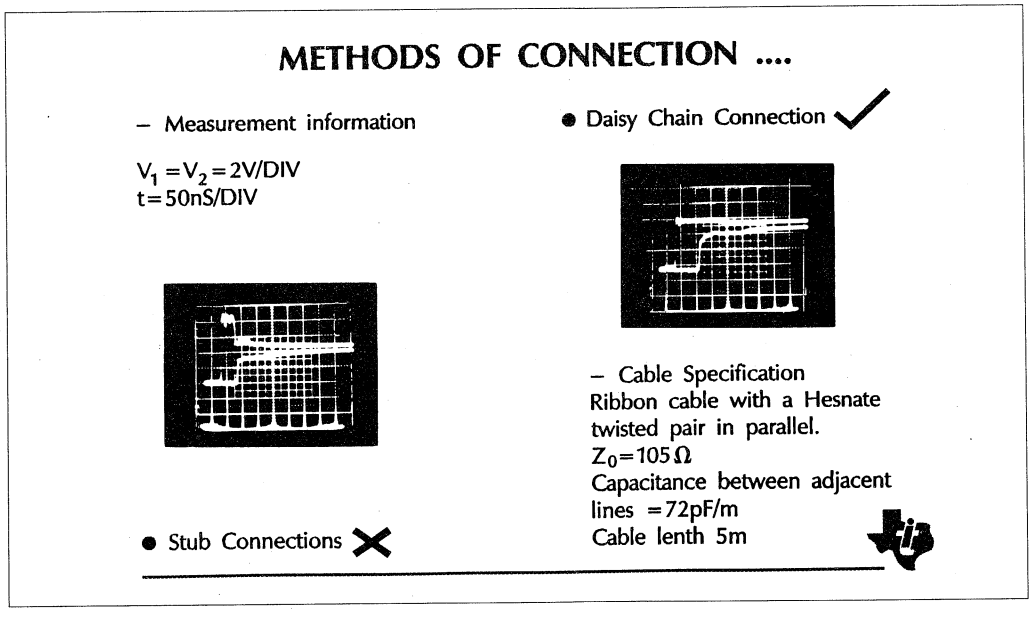


Figure 13- Methods Of Connection

This foil shows a comparison of the daisy chain connection method to the star connection.

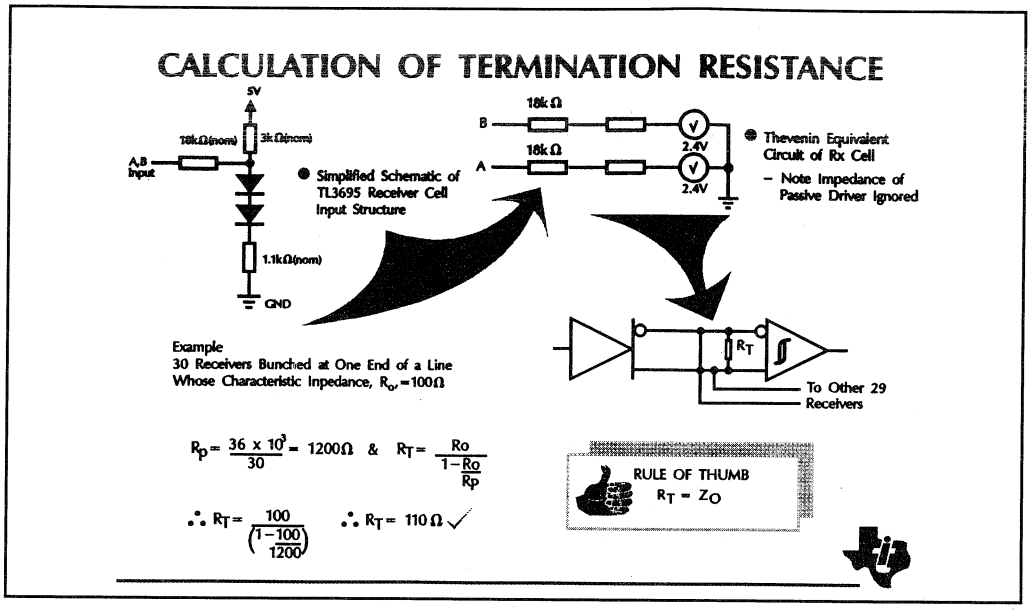


Figure 14- Calculation of Termination Resistance

Another important factor in data transmission with fast edges and high data rates is the termination of the transmission line itself. For better performance the line will need to be terminated by a resistor of a value close to its characteristic impedance. This can become somewhat confusing when taking the receiver's input impedance into account, especially when many receivers are grouped together at the far end of the line.

Each input of the receivers has a nominal input impedance of 18kΩ feeding into a diode-transistor- resistor biassing network, providing a thevenin equivalent of an 18kW input resistor tied to a common mode voltage source of 2.4V. It is this configuration which provides the large common range of the receiver required for RS-485 systems.

Due to the fact that the each input is biassed to 2.4V, the normal common-mode voltage of balanced RS-485 systems, the 18kΩ resistors on the inputs can be taken as being in series across the input of each indivual receiver.

If thirty such receivers are placed close together at the end of the line, they will tend to react as thirty 36kΩ resistors in parallel with the termination resistor. This overall effective resistance will need to be close to the characteristic impedance of the line.

The effective parallel receiver resistance, R_p, will therefore be equivalent to;

$$R_p = 36 \times 10^3 / 30 = 1200\Omega .$$

While the termination resistor, R_T, used will be equal to;

$$R_T = Ro / [1-Ro/R_p] .$$

Thus with a line with characteristic impedance of 100Ω means that the termination resistor R_T should be:

$R_T = 100/[1 - 100/1200] = 110\Omega$

So re-iterating the termination resistor R will normally be equal to the characteristic impedance, Z_o, and even in conditions of extreme loading the R_T value required will not significantly varry from Z_o.

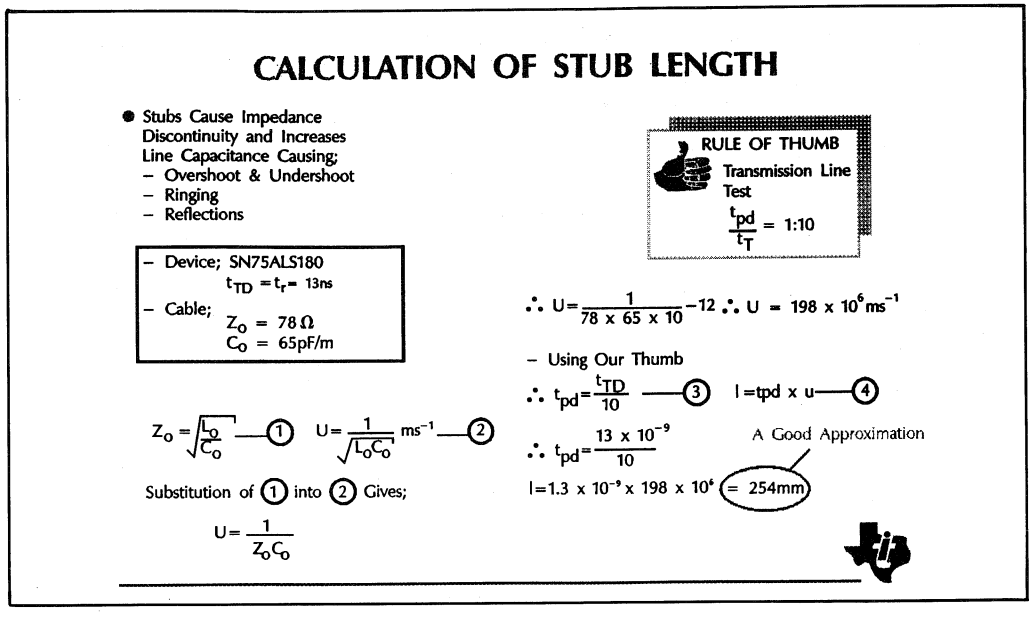


Figure 15- Calculation of Stub Length

When using transmission lines ultimately some connections will be needed to connect devices to the line, furthermore these connections must result in minimal distortion to the line signal. A distortion could be both amplitude and phase distortion producing reflections amongst other elements.

These connections are usually termed stubs. A stub is a short connection between the transmission line and driver or receiver. But being a parallel connection from the transmission line it itself, if excessively long, it too could be considered as a transmission line causing distortion due to a change in impedance on the line and reflections from the end of the stub.

To minimise these effects the stub should be kept as short as possible, and should be seen as a lumped (non transmission line) rather than a distributed (transmission line) load to the incident voltage.

How Short is Short ?

It has been described earlier that a pair of cables will act as a transmission line if the round trip propagation delay, 2tpd ,is more than 5 times the transition times of the driver, t_T. The converse is true if the line is not to operate as a transmission line but as a lumped parameter shunt.

The foil shows a calculation for determining the maximum length of the stub.
Our rule of thumb means that the transition time of the pulse sent down the line should take

ten times the time taken for the pulse to propagate to the end of the stub. Meaning that any reflections will be encorporated into the transition edge, ie not a transmission line.

From this basis the length of a stub can be calculated using the cable and driver parameters.

The pulse speed down the line, U, equals the reciprocal of the product of the line impedance and line capacitance, both of which are normally specified for the cables used. This can be inverted to give us the cable delay per unit length, t.

The propagation delay down the stub should be at the most one tenth of the transition time of the pulse. These can be brought together to give the length of the stub, l , as;

$$l = u \times t_T / 10$$

So using the SN75ALS180 and its transition time of 13ns with a cable of charateristic impedance 78Ω and line capacitance of 65pF, gives a maximum stub length of 254 mm or ten inches.

The main effect that the line will see is an increase in the capacitance of the line.

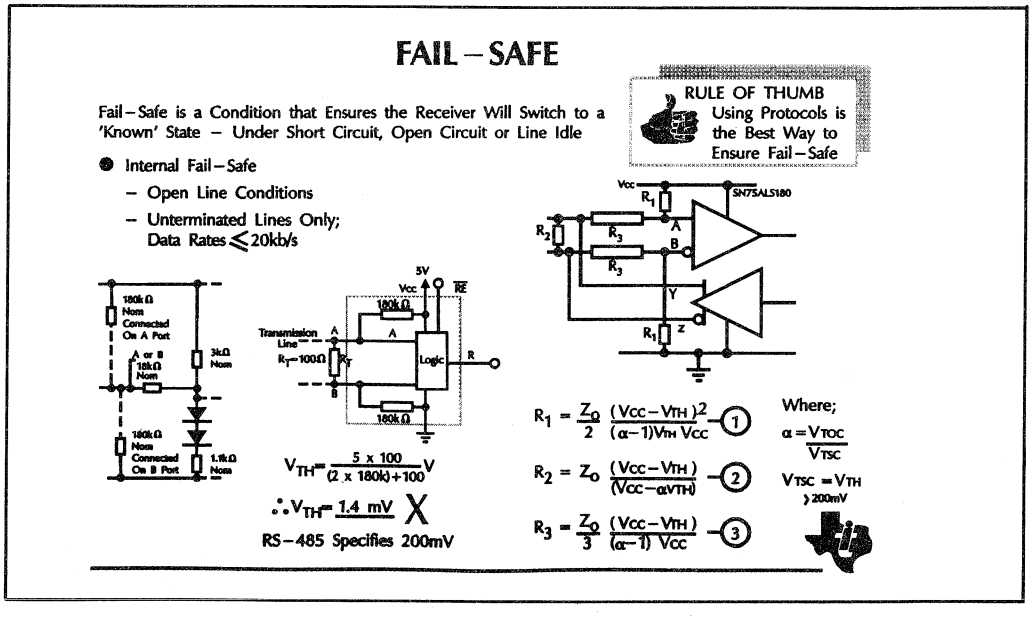


Figure 16- Fail Safe

In any party line system it is likely that, at any one instance, all drivers could be in in the high impedance state, thus leaving the bus floating, line idle. A receiver should be able to detect this situation and place its output in a known state thus preventing any spurious information from being processed.

There are several ways to prevent this from occuring, including the use of line bias resistors and protocols. Protocols are however the prefered approach. Termed *fail -safes* these ideally should define the reciver into a known state for line short circuit conditions also.

Several manufacturers include internal fail-safe protection in the receiver input circuit. However this only affords protection against open circuit line conditions and even then only for unterminated lines. This limits its usefulnes to lines with data rates less than 20kb/s.

T.I.'s SN75ALS176 transceivers along with other ALS devices contain internal passive pull-up resistors, of the order of 180kΩ. These resistors provide open circuit unterminated line definition but when the line is terminated the voltage they generate across the line reduces to about 1.4mV. Large value resistors are used to minimise the power consumed by the resistors. When operating at lower data rates the line can often go unterminated, and so this open circuit fail-safe will suffice.

For open circit fail-safe at higher data rates external line bias resistors can be used, while R_3 is shorted out. However the overall resistance value must result in a value equal to the characteristic impedance of the line. The resistor values for such a termination is calculated below;

The effect of the pull-up and pull-down resistors, R_1, are that they will appear to be summed together in parallel with the termination resistor, R_2.

This means that the characteristic impedance, Z_o, equals;

$$Z_o = R_2 \times 2R_1 / [R_2 + 2R_1]$$

The voltage across the line, V_{TH}, will be;

$$V_{TH} = V_{CC} \times R_2 / [R_2 + 2R_1], \text{ combining these two gives;}$$

$$R_1 < 0.5 \times Z_O \times [1 + V_{CC} / V_{TH}] \quad \text{and,}$$

$$R_2 = Z_O [1 + V_{TH}/V_{CC}]$$

`Reducing R_1 will increase the threshold voltage thereby increasing the noise rejection when the line is high impedance.

`For systems requiring both open and short circuit fail safe resistors R_3 must be included, as shown in the foil.

`In order to effect short circuit fail safe a tranceiver with separate receiver inputs and driver outputs is required, e.g., SN75ALS180. Otherwise R_3 will adversely load the driver output of a transceiver connected device (common driver output and receiver input).

`Again the incident voltage see's R_2 in parallel with the two pull-up/pull-down resistors, but it will also see two R_3 resistors in series with $2R_1$.

$$Z_O = \frac{2 R_2 \times (R_1 + R_3)}{2 R_1 + (R_2 + 2R_3)} \qquad \text{(a)}$$

The short circuit threshold voltage across the line, has to be greater than the minimum specified by the standard, 200 mV, and will be;

$$V_{TSC} = V_{TH} = \frac{2R_3}{2R_3 + 2R_1} \times V_{CC}$$

$$= \frac{R_3}{R_1 + R_3} \times V_{CC} \qquad \text{——— (b)}$$

The open circuit threshold voltage across the line, V_{TOC}, will be greater than V_{TSC} and will be greater than the minimum specified by the standard by a factor ;

where $\alpha = \frac{V_{TOC}}{V_{TSC}}$

$$V_{TOC} = \frac{R_2 + 2R_3}{2R_1 + R_2 + 2R_3} \times V_{CC} \qquad \text{——— (c)}$$

subsituting (b) into (a) and (c) and making R_1 , R_2 , R_3 the subject of the formula gives equations which provide both short circuit and open circuit fail safe.

$$R_1 = \frac{Z_O}{2} \frac{(V_{CC} - V_{TH})^2}{(\alpha - 1) V_{TH} V_{CC}} \qquad \text{——— (1)}$$

$$R_2 = Z_O \frac{(V_{CC} - V_{TH})}{(V_{CC} - \alpha V_{TH})} \qquad \text{——— (2)}$$

$$R_3 = \frac{Z_O}{2} \frac{(V_{CC} - V_{TH})}{(\alpha - 1) V_{TH}} \qquad \text{——— (3)}$$

where; $\alpha = \frac{V_{TOC}}{V_{TSC}}$ and $V_{TSC} = V_{TH} > 200$ mV

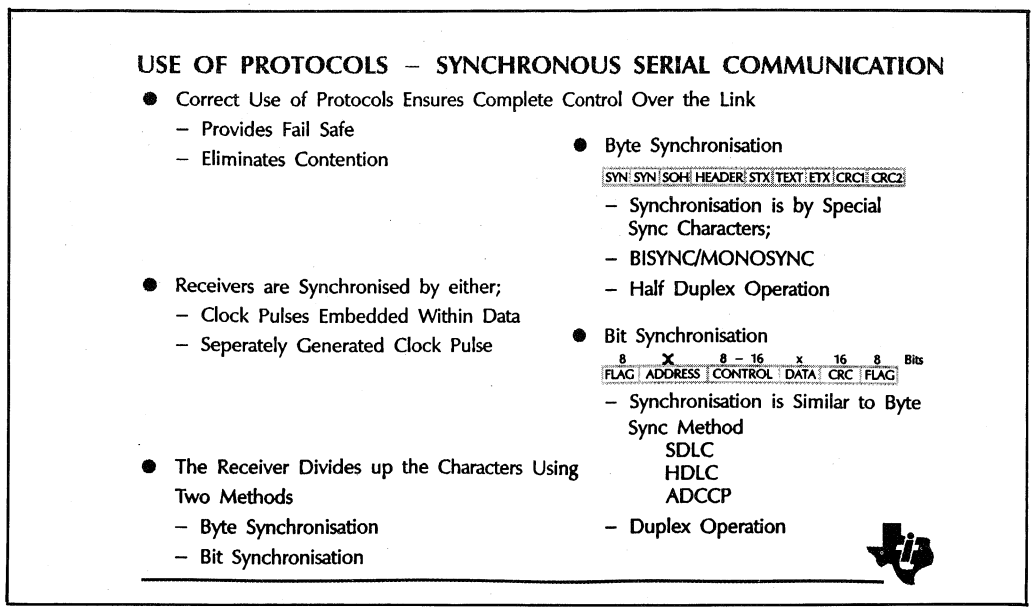


Figure 17- Use of Protocols- Synchronous Serial Communication

As discussed previously using line terminations to effect a fail-save is not a recommended practice, however what is recommended is the use of protocols. Protocols come in many forms (two of which are explained below) and provide a set of rules which defines the meaning and order in which data should be sent. In particular they can be used to provide a fail safe feature and be used to avoid contention. Contention occurs when several drivers try and address the link at once. This can lead to high currrent sinking or souring leading to excessive thermal dissipation in the drivers. Fail-safe is ensured by allowing the receiving station to respond to valid data only, this is achieved by sending a preamble before each data packet . The preamble consists of a pre-determined pattern of bits, which signals to the receiver that data is about to follow. Anything other than this preamble should be ignored by the receiver.

Party Line Protocol Formats

Party line applications uses either half duplex or full duplex transmission. Half duplex transmission mode is where a driver and receiver can communicate with each other bi-dirrectionally over the same link, they cannot transmit similtaneously. A party line transmission line format can be achieved using half duplex by multiplexing between a number of driver / receiver pairs. Full duplex communications involves the simultaneous, two way flow of data from driver / receiver pairs.

A communication line operated in a multiplex operation such as the half duplex party line system reduces wiring costs when compared to the simplex operation (simplex one driver for one receiver). Only one line is needed to implement the communication system, though control of the multiplexing does require complex protocol or hanshaking circuits.

A typical (simplified) a protocol sequence would contain the following elements;

i) Driver requests access to communication link (bus)
ii) Link controller responds to request and gives go ahead when bus is free
iii) Driver gains bus mastership and sends data which is precede by a destination code
iv) Receiver sends an acknowledge
v) Driver receives confirmation and releases the bus

Synchronisation

Some form of synchronisation is necessarry for the receiver to determine the start and finish of the received bits. Two schemes, with many variations, are adopted ; *Asynchronous and synchronous.*

Asynchronisation, or start stop bit communication, uses a system where characters are sent one at a time without necessarily having any fixed time relationship between each other. In such a case the driver sends start bits followed by the information field, followed by one or more stop bits. This used to inform the receiver that information data will follow the start bit and will end prior to the stop bit. The data is usually broken into small chunks of 8-bits, one byte, which is proceeded with a start bit and concluded with a stop bit. This is one of the schemes employed by RS-232.

Synchronous transmission is used to transmit complete blocks of data at one time.In synchronous transmission the duration of each bit is the same. With all characters being the same length the receiver only has to identify the first character and then clock the others in at a predetermind rate.

Serial synchronous communication uses a similar scheme and either embeds the timing information in the data or provides a seperate clock signal. However the bit steam still has to be divided up into the individual characters. There are two main methods of achieving character synchronisation: *Byte synchronisation and bit synchronisation.*

Byte synchronisation, one of the first sycnchronous methods to be introduced is best known by IBM's bisync and monosync . Synchronisation is achieved by using special SYNC characters which are transmitted in between data packets. The receiver continually monitors this transmission and uses it to synchronise itself . After receiving one (monosync) or two (bisync) sync pulses the receiver is said two be in the synchronised mode and is ready to receive data. Synchronisation is ensured by re-sending the sync bits every few hundred characters, for this reason data is grouped together in frames or packets which start with sync characters. Each frame is 8-bits long

The bisync protocol also defines a structure for a frame that includes control information and error checking capability. The foil shows the basic frame structure with the sycn characters followed by the header field. *SOH* identifies the begining of the *header* block .The header field is user defined and generally contains control specific information such as rest data link, message numbering priority ..etc. Start of text, STX, identifies the end of the header field and defines the beging of the text field . The text or data field contains application specific information which must be sent to the application controller intact. ETX, signals end of text and CRC1 and CRC2 are used as cyclic redundancy check bits. Notice that STX, ETX etc are the standard ASCII control codes. Bysnc is essentially a half duplex system because each

frame requires an acknowledge from the receiver before commencing with the next frame. Obviously sending acknowlege codes back and to reduces the data rate, to overcome this bit synchronisation was developed.

SDLC (synchronous data link control) , again made popular through IBM , was one of the first bit synchronisation protocols available. The CCITT also adapted this standard for their high level data link (HDLC) protocol. Both are very similar to the CCITT X25 layer 2 packet switching local area networking standard. Initially bit sync looks very similar to byte sync , ie during data null periods sync pulses are sent over the link to synchronise the receiver and driver. However after the sync period the data may be grouped in any number of bits. Byte-sync systems are resricted to 8-bit packets.In the SDLC and HDLC messages are formatted into frames with each frame being divided into fields. The start flag is the sync data while the address field contains the destination address to select the required receivers. The control field can be configured as either an information field or supervisory field. The information field, which is the usual format, contains status information on the number of frames sent or received. Data field follows and contains application specific code.The supervisory or management frame is used to acknowledge successful receipt of data. CRC is used for error checking and flag is the next sync signal.

Party Line Considerations

The following points should be considered for correct party line operation;

i) Each driver must have a tri-state, two logic states and a high impedance mode. Also at any one instance it is likely that all drivers could be in in the high impedance state, thus leaving the bus floating. A receiver should be able to detect this situation and protect agains any spurious information.

ii) Receivers may oscillate if left unconnected causing other used receivers in the same package can be affected. Therefore it is recommended that all unused receiver inputs should be tied to defined logic states.

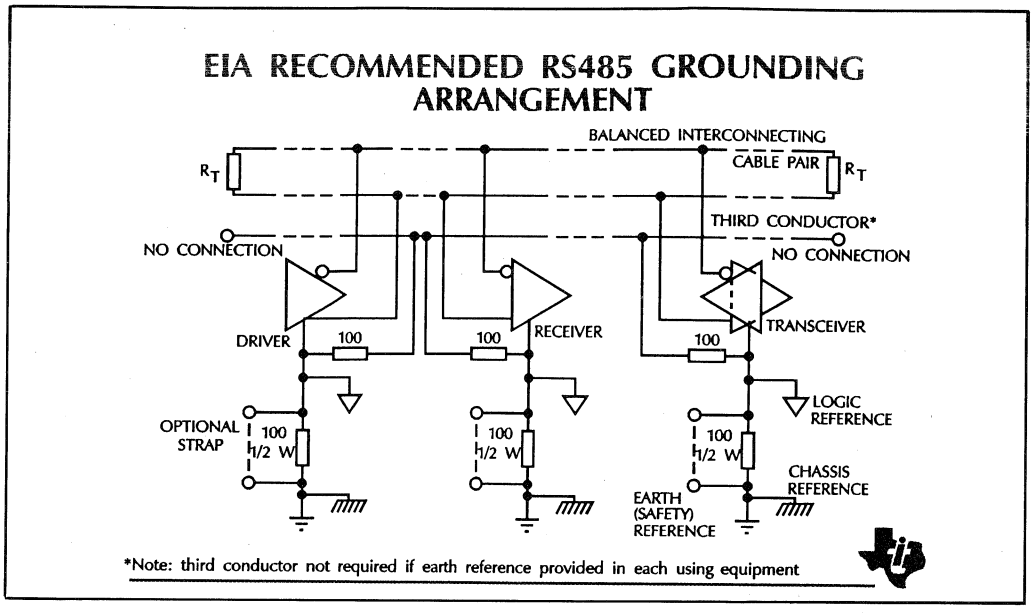


Figure 18 - EIA Recommended RS485 Grounding Arrangement

This foil shows the grounding arrangement recommended for the EIA RS485 specification. The specification states that; "proper operation of the generator and receiver circuits requires the presence of a signal return path between the circuit grounds of the equipment at each end of the interconnection . The circuit reference may be established by a third conductor connecting the common leads of the devices, or it may be provided by connections in each using equipment to an earth reference.

The grounding arrangements are shown in the foil. When the circuit reference is provided by a third conductor, the connection between circuit common and the third conductor must contain some resistance (eg 100 Ω) to limit circulating currents when other ground connections are provided for safety".

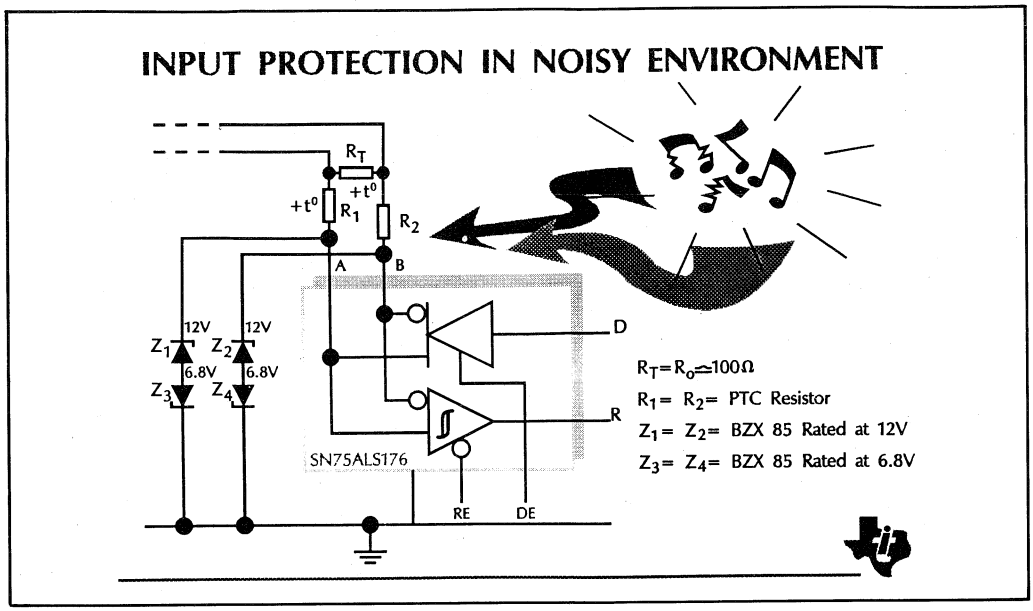


Figure19 - Input Protection in a Noisy Environment

Often when sending data over long distances or in electrically hostile environments, ie factory automation, the noise immunity afforded by the differential line is not enough and extra help is needed. This foil shows how external diodes offer transient spike protection to the SN75ALS176 RS-485 transceiver.

R_T is the usual termination resistance which is equivalent to the characteristic impedance of the line. R_1 and R_2 are positive temperature coefficient, PTC, resistors which present minimal load to the driver under normal operating conditions. Under fault conditions their resistance value rises to provide current limiters for the diode chain.

Z1 and Z2 are chosen to protect the input from positive spikes greater than 12 V whilst Z3 and Z4 protect the device from negative going spikes greater than 6.8 V.

linear circuits and the need to seperate 'noisy' digital grounds from 'quiet'

	No. of drivers	No. of Receivers	Propagation Delay t_{PLH}, t_{PHL} Dx(t_{DD})	Rx	Skew Dx	Rx	Diff O/P transition time (t_{TD}) Dx	Icc
SN75ALS176	1	1	13ns	19ns	6ns	6ns	13	30mA
TL3695	1	1	22ns	37ns	8	8	18	50mA
SN75ALS180	1	1	13ns	19ns	6	6	13	30mA
SN751177	2	2	25ns	35ns	–	–	35	110mA
SN751178	2	2	25ns	35ns	–	–	35	110mA
SN75ALS193	–	4	–	22ns	–	–	–	35mA
SN75ALS195	–	4	–	22ns	–	–	–	35mA
SN75ALS194	4	–	14ns	–	6ns	–	14ns	45mA
SN75ALS192	4	–	14ns	–	6ns	–	–	45mA
SN75ALS197	–	4	–	22ns	–	–	–	35mA
SN75ALS199	–	4	–	22ns	–	–	–	35mA
SN75ALS170	3	3	13ns	19ns	6		13	90mA
SN75ALS171	3	3	13ns	19ns	6		13	90mA

Figure 20 - Products for EIA - RS422 and EIA - RS485

Texas Instruments have an extensive range of devices in support of both EIA-RS422 and EIA-RS485 standards.

The range comprises: drivers, receivers and transceivers. The EIA-RS422 family includes industry standard devices such as AM26LS31, through to the high performance offered by the SN75ALS19X family. The EIA-RS485 range is similarly well supported, including familiar devices like the SN75174 and the high performance SN75ALS176.

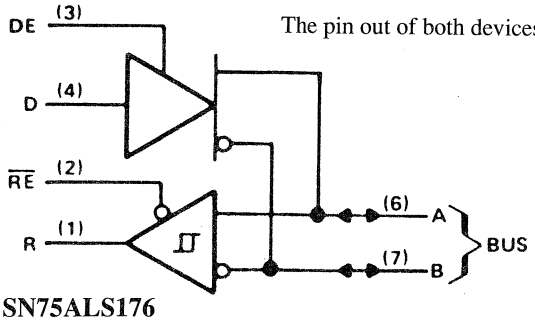
Devices of note are shown in the above figure, of particular interest is the range of advanced low-power Schottky devices; SN75ALS176 and SN75ALS180. A brief description of these devices is given below:

The SN75ALS176 and SN75ALS180 are monolithic integrated circuits designed for bi-directional data communication on multipoint bus transmission lines. The SN75ALS176 is a single differential transceiver while the SN75ALS180 is a single differential driver/receiver pair.

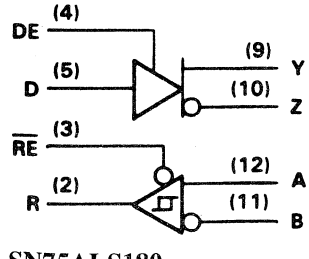
The SN75ALS176 combines a three-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be extremely connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus.

The SN75ALS180 combines a 3-state differential line driver and a differential input line receiver both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected to separate pins for greater flexibility and are designed to offer.

The pin out of both devices is shown below:



SN75ALS176



SN75ALS180

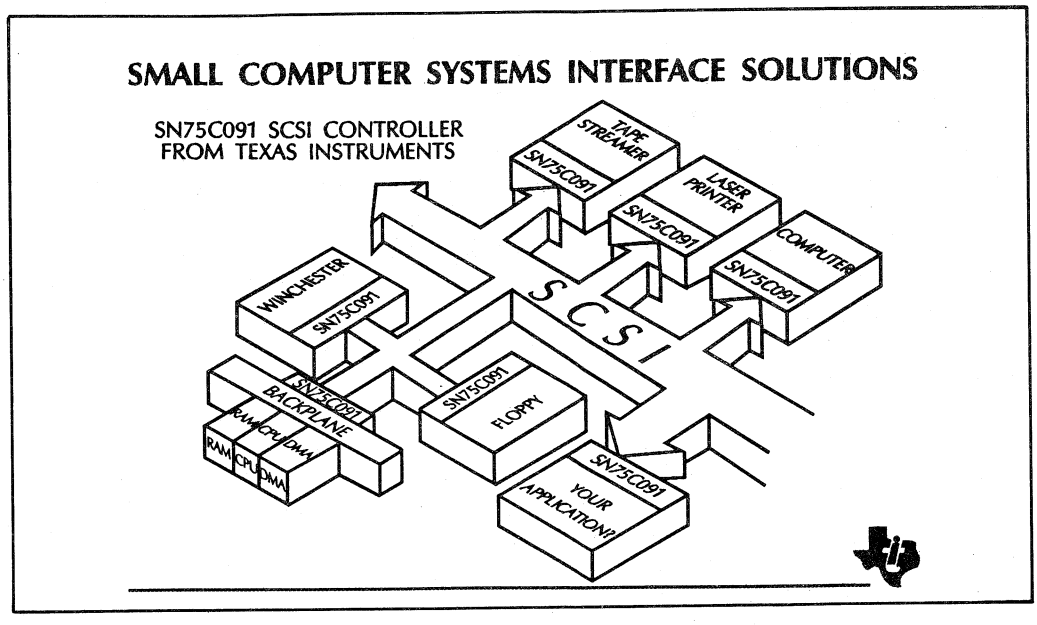


Figure 1 - Small Computer Systems Interface Solutions

SCSI interface can be used to connect computers, disk drives, optical storage devices, laser printers, scanners, tape drives etc. together using a common bus system. Moreover the standard specifies the mechanical, electrical and functional requirements for a small computer input/output bus interface and command sets for intelligent peripheral device types, particularly storage devices commonly used with small computers.

The SCSI Advantage

SCSI offers advantages to both the equipment user and the equipment vendor. Users benefit from increased system performance and a wider choice of compatible peripherals available 'off the shelf, which are not system specific. Vendors benefit by not having to design individual interfaces for each different disk drive or peripheral that they supply. Standardisation between manufacturers increases the size of the potential market for the product.

SCSI is capable of supporting communication between multiple computers as well as computer to disk drive for example. Also disk to disk data transfers can take place which execute completely independently from computers on the bus. The bus is therefore 'intelligent'. This is one of the prime reasons for an intelligent I/O bus, like SCSI, to off-load some of the more mundane but time intensive I/O cycles from the host CPU.

A Brief History of SCSI

SCSI has been an official ANSI standard since 1986 (X3.131-1986), however its roots go back much earlier to the IBM mainframes of the early 1960's. *(ANSI stands for American National Standards Institute, which has been responsible for such international standards as the ASCII 7-bit data code.)*. The early IBM 360's had a byte-wide I/O bus known as the block *multiplexer channel* which had the capability to communicate with several peripherals at once. The IBM bus, also known as the *OEM channel* , soon became the defacto interface standard for

peripheral manufactures. However it was realised that this was fast giving IBM an unfair competetive advantage over other computer manufacturers. Consequently in the early 1980's ANSI began work on a non-propriety bus called IPI , Intelligent Peripheral Interface. This was infact a superset of IBMs' OEM channel. Concurrent with this development Shugart Associates (a disk drive manufacturer) were working on a flexible I/O interface. This interface known as the SASI (Shugart Associates System Interface) soon became adopted by many major OEM's, leading to its natural adoption by ANSI. This fitted well ito ANSI's portfolio who now had a high performance I/O standard in the guise of IPI and a lower performance standard in SCSI. However with the advent of SCSI-2 the difference between IPI and SCSI has diminished.

SCSI Specification

SCSI is implemented on a 50 way bus made up of data-bits, parity-bit, ground lines, power line and control lines. The data lines are used to transfer data, command status and message information. While the control lines provide the necessary sequencing and handshaking information to control the flow of information. The number of pins used depends upon whether differential or single ended SCSI is being implemented, SCSI supports both. Differential SCSI offers the highest noise immunity and allows for transmission upto 25 metres, differential SCSI conforms to the EIA-RS485 specification and is generally recommended for cabinet to cabinet links. Differential SCSI uses all 50 lines where many of the odd-numbered pins form the differential signals with the corresponding even-numbered pins. Single ended SCSI is less immune to noise and consequently is used for shorter distances, upto 6 metres, this usually limits it to inter-cabinet communications. In a single ended system all unused odd-numbered pins are grounded (except pin 25) to provide additional shielding between the signal lines, see figure 1.1 for details of SCSI pin assignments.

SIGNAL	PIN NUMBER	PIN NUMBER	SIGNAL
SHIELD GROUND	1	2	GROUND
+DB(0)	3	4	-DB(0)
+DB(1)	5	6	-DB(1)
+DB(2)	7	8	-DB(2)
+DB(3)	9	10	-DB(3)
+DB(4)	11	12	-DB(4)
+DB(5)	13	14	-DB(5)
+DB(6)	15	16	-DB(6)
+DB(7)	17	18	-DB(7)
+DB(P)	19	20	-DB(P)
DIFFSENS	21	22	GROUND
GROUND	23	24	GROUND
TERMPWR	25	26	TERMPWR
GROUND	27	28	GROUND
+ATN	29	30	-ATN
GROUND	31	32	GROUND
+BSY	33	34	-BSY
+ACK	35	36	-ACK
+RST	37	38	-RST
+MSG	39	40	-MSG
+SEL	41	42	-SEL
+C/D	43	44	-C/D
+REQ	45	46	-REQ
+I/O	47	48	-I/O
GROUND	49	50	GROUND

Figure 1.1 Differential SCSI pin Assignments

As well as providing for differential or single ended communication the SCSI bus can operatie in either asynchronous or synchronous mode. Asynchronous mode allows transfers of upto 1.5 Mbytes/sec whilst in synchronous mode transfer rates of upto 4 Mbytes/sec are permitted.

How Many Peripherals ?

SCSI can support upto eight peripherals (including the master). Each peripheral can in turn support a further 8 logical units, which can drive upto 256 logical subunits. Thus a total of 14,000 peripherals can be supported on one SCSI bus if there is one host and each peripheral is a logical subunit.

Texas Instruments supports the SCSI standard with the SN75C091 controller I.C. Each peripheral in a SCSI system is fitted with a SCSI controller which is responsible for passing information from the SCSI bus across to the host uP bus or control electronics in the peripheral. The SCSI controller ensures that all data transfers and bus communications take place as per the SCSI protocol.

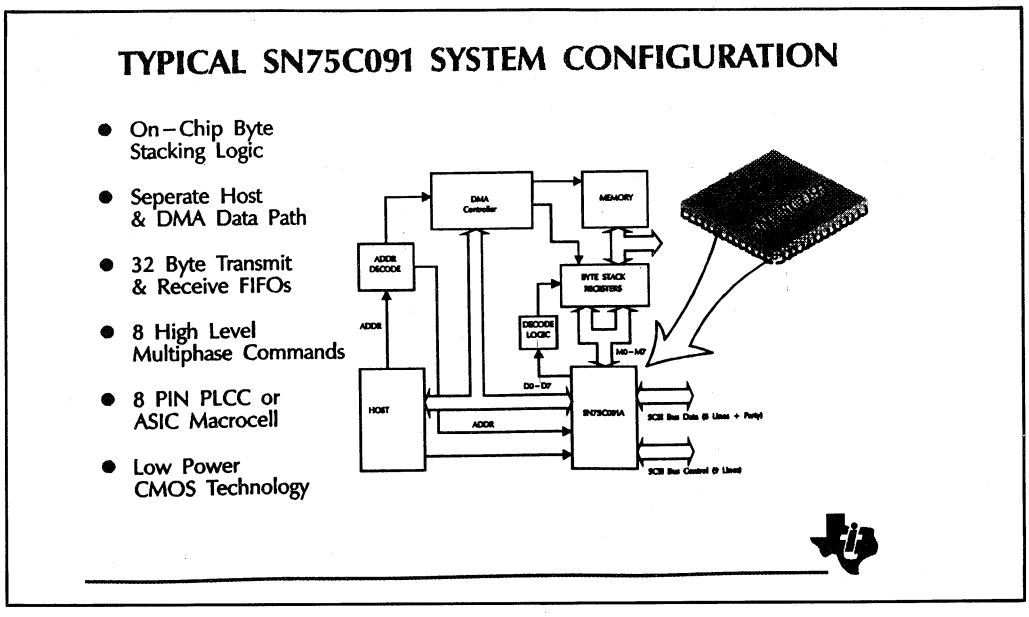


Figure 2 - Typical SN75C091 system Configuration

Before a typical SCSI implementation can be discussed it is neccessery to have a basic understanding of the SCSI signal lines and the bus phases. Ths is best attempted by dividing the standard up into its two main areas, the physical layer and the logical layer.

Physical Layer

The physical layer sets a standard for the interconnection of the SCSI devices. All devices must be daisy chained together using a common 50 way cable, since the signal is half duplex both ends of the bus must be correctly terminated. Differential and single ended systems may not be used on the same bus.

Logical Layer

This contains information on the protocol and timing aspects of the SCSI interface. The SCSI bus operates in a series of distinct transactions , known as bus phases, at any one time

the SCSI bus must be in one of these states. The phases determine the direction and content of the data lines. The eight possible phases are; *Bus free, arbitration, selection, reselection, command, data, status and message.* Arbitration is optional although it is implemented by most
controllers, the SN75C091 for example. The sequencing and handshake information to control the transition between phases is handled by the 9 control signals,

The phase diagram in figure 2.1 shows the relationship between these phases. The SCSI has no bus master, ie the usual master/slave aruguement is not true as in theory each peripheral as well as host controllers can act as either initiators or targets.

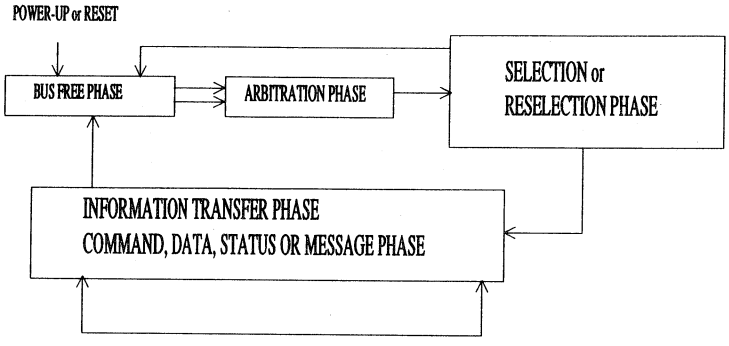


Figure 2.1 SCSI Bus Phase

BusFree. All sequences begin in the bus free phase, this is the only phase in which the BSY signal is not inserted and indicates that no modules have control of the bus.

Arbitration. In this phase all potential masters on the bus compete for bus ownership. The phase begins when an initiator attempts to gain control of the bus by asserting its BSY signal and sets its data bits to correspond with its SCSI ID. The highest ID wins and the others back off permitting the now bus master to continue his transaction by asserting the SEL signal .

Selection / reselection. The arbitration phase is followed by the selection or reselection phase. Here the initiator selects a target by placing the targets ID and its own ID on the bus (while SEL is asserted) and releases BSY. If the target is valid it responds by asserting BSY allowing the initiator to release SEL.

Command phase is now entered which is now controlled by the target. The reselection phase occurs when a target wins the arbitration and re-establishes contact with an initiator that had previously sent it a command. The control signals used in this transaction are the C/D, I/O, REQ, ACK and MSG, the combination of signals is best explained in figure 2.2.

MSG	SIGNAL C/D	I/O	PHASE NAME	DESCRIPTION
0	0	0	DATA OUT	Initiator sends data to target
0	0	1	DATA IN	Target sends data to initiator
0	1	0	COMMAND	Initiator sends status to initiator
0	1	1	STATUS	Target sends status to initiator
1	0	X		(Reserved)
1	1	0	MESSAGE OUT	Initiator sends message to target
1	1	1	MESSAGE IN	Target sends message to initiator

Figure 2.2 Information transfer phases and SCSI control signals

In the command phase the target requests a command from the initiator, either data in, data out, status, message in or message out. The data-in and data-out phases are self explanatory, in the status phase the target sends a status byte indicating the success or failure of a command. Message in and message out are used to pass messages between the communicating modules. Typical messages could include; command complete or initiator detected error.

Thorough discussion of the SCSI transactions is beyond the scope of this seminar. However there are numerous articles, data sheets and the standard itself which provide valuable sources of information.

The block diagram demonstrates how a typical SCSI bus can be implemented using TI's SN75C091. This particular implementation uses seperate 091 DMA port and 091 host bus port. Whilst seperate DMA and host ports are not always required they are a necessery feature for high speed transactions. For example whilst the DMA could be actively transfering data the host port could be used for conveying status information to the host. The diagram does not show all of the chip connections. For instance, DMA request lines are not shown. (This simplifies the diagram.) Other key features of the SN75C091 are as folows;

0 On-chip byte stacking logic for easier interfacing to 16,24,32 bit host bus.

0 Seperate data paths for host bus and DMA bus.

0 32 byte deep transmit and receive FIFOs with parity bit.

0 8 high level multiphase commands, minimizes processor interrupts.

0 68 pin PLCC package or ASIC macrocell.

0 Low power CMOS technology.

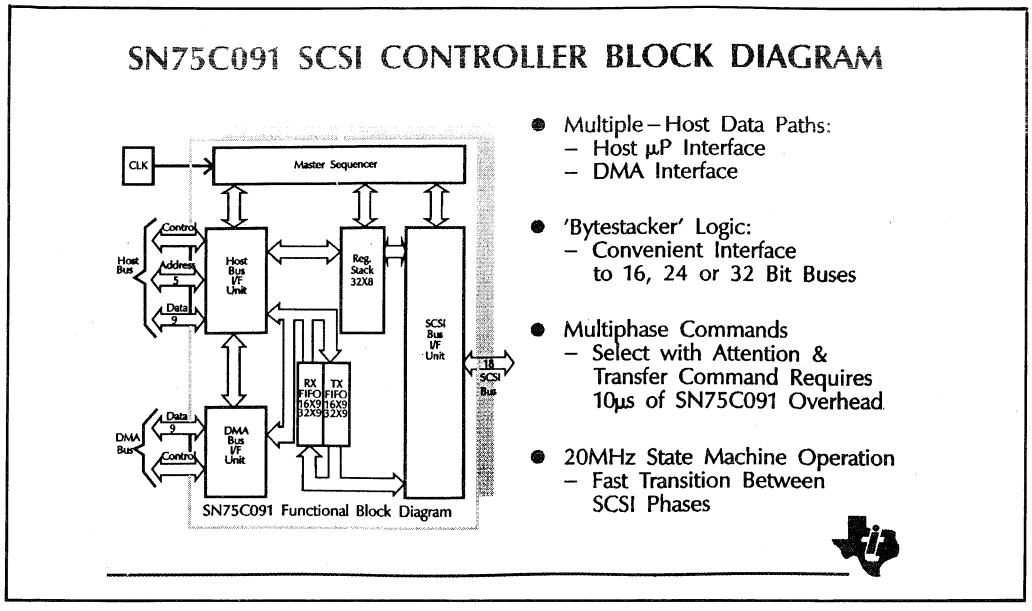


Figure 3 - SN75C091 SCSI Block Diagram

This foil shows the internal architecture of the SN75C091A and serves to highlight several key features.

0 **Seperate interface ports for host uP databus and host DMA bus.** Seperate data ports are not always required but in a high speed system the DMA port could be transferring data continuously, whilst at the same time the host uP could be interrogating the SN75C091 controller for status information.

0 **On-chip 'bytestacker' logic.** This is a novel feature that is designed to make it easier to interface to host backplanes with 16, 24 or 32 bit wide buses. The SN75C091 actually generates the decoding signals necessary to control external latches that are used to multiplex the 16 , 24 or 32 bit host bus down to the 8 bit needed by the S75C091.

0 **Multiphase commands.** For example the SN75C091 can complete a select with attention and transfer command within 10µs.

A comprehensive set of 'multiphase' commands exist: Commands are passed across to the SCSI command register from the peripheral driver software resident in the host system. These commands are of two types; interrupting & non-interrupting. As their names imply, they differ in whether or not an interrupt is generated to the host to indicate completion of the command. Non-interrupting commands omplete within a few clock cycles. Interrupting commands take from ten to several thousand clock cycles. The interrupting commands are further divided into two subsets, single phase & multi-phase commands. Single phase commands generally only execute one (or more) SCSI bus management phase or one info phase eg. arbitration & selection, data transfer phase or send command phase. An interrupt is generated at the completion of the command.

The multiphase commands usually include at least one information transfer phase and one or more bus management phase. They can therefore be thought of as high level commands that group together several smaller commands into one instruction.Interrupts are handled internally to the '091 during execution of the multiphase commands. This reduces the overhead of the host processor. For example, the multiphase command 'select with attention & transfer, is a single command that represents a very common SCSI sequence ie. bus arbitration, target selection, send ID message, send SCSI command, send or receive data, receive status, and receive a command complete message.This command only requires a total of 10 µs of SN75C091 processing time (assuming an infinitely fast target response). This is due to the fast state machine design which operates at 20 MHz. Many competition parts use processor type structures which have to clock through their SCSI instructions at a slower pace.

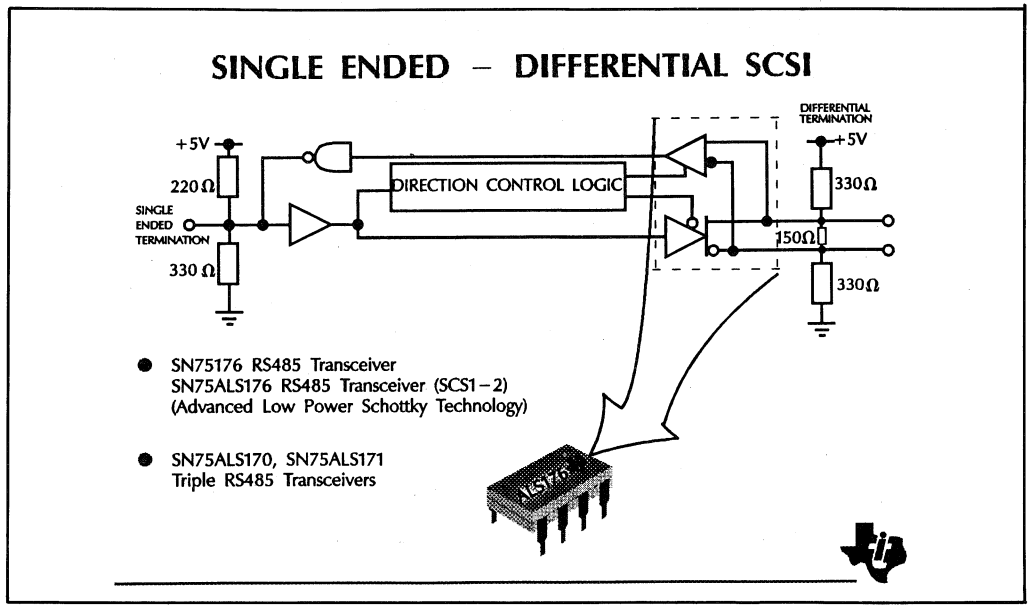


Figure 4 - Single Ended to Differential SCSI

As briefly mentioned earlier, differential SCSI is often desirable for driving longer line lengths (ie cabinet to cabinet) or where niose interference is a potential problem. Unfortunately most controllers only have single ended drive capability, this foil shows how a single ended output can be converted to a differential output.

The advanced low power schottky series of RS-485 devices are instrumental in effecting this conversion. Further more their low power and high speed capability make them ideal for SCSI operation. The SN75ALS176 is a single transceiver housed in an 8-pin package, with a maximum data rate capability of 23 Mb/s. The SN75ALS170 and SN75ALS171 are triple versions with different enabling schemes allowing for half duplex and full duplex operation.Single ended implementations of SCSI usually incorporate the required 48mA drivers on the SCSI chip itself). Some SCSI chips are designed for differential bus operation (without 48mA drivers) and require interfacing to RS485 drivers and receivers. SN75ALS176 is particularly useful due to its high speed of operation, (full imlimemtation requires eighteen '176 type devices) SN75ALS176 is also recommended for SCSI-2 systems which are required to operate at upto 10 Mbits/sec.

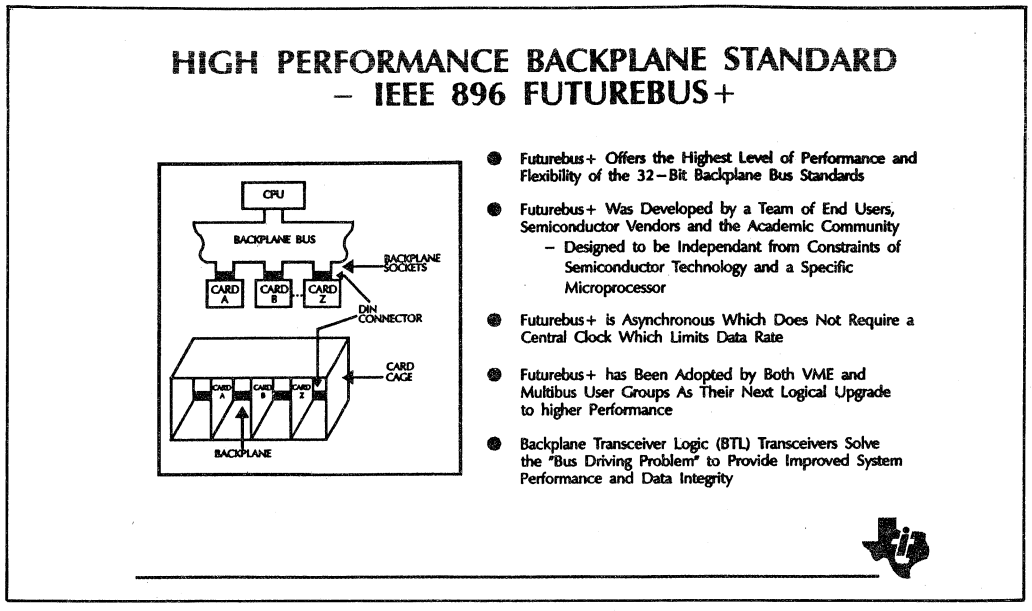


Figure 1 - High Performance Backplane Standard - IEEE 896 Futurebus+

What is Futurebus+?

The following serves as a brief overview to the topic of Futurebus+, further comprehensive material is available in the form of data sheets, magazine articles and the IEEE 896 standard itself.

Futurebus+, is a high performance backplane allowing, as all backplanes, option cards, or daughter boards to communicate with each other via the backplane. Before further discussion of the Futurebus+ standard itself, let's discuss the backplane environment and more importantly why yet another backplane standard is neccessary;

The backplane is the primary interface between option cards in the PC card frame. It is the main communication highway, handling data, control and address signals. It allows the CPU to address option memory, I/O cards, co-processors, LAN adaptors, and graphics adaptors etc. As is the case when multi-vendors, both PC manufacturers and add-on builders, are involved standardisation is necessary. Standardisation provides system designers a clear unambiguous standard to follow during the design phase.

Limitations of the Current Backplane Standards

There are many backplane standards around, both proprietary and non-proprietary. In addition to the general PC/AT buses like EISA/MCA there are many higher performance standards which are optimised for multiprocessing. Such standards are Multibus II, Q bus, VMEbus, NuBus and PI-Bus. Applications range from the humble desk top PC to test equipment, and graphical workstations for CAD/CAM. The market split is shown in figure 1.1.

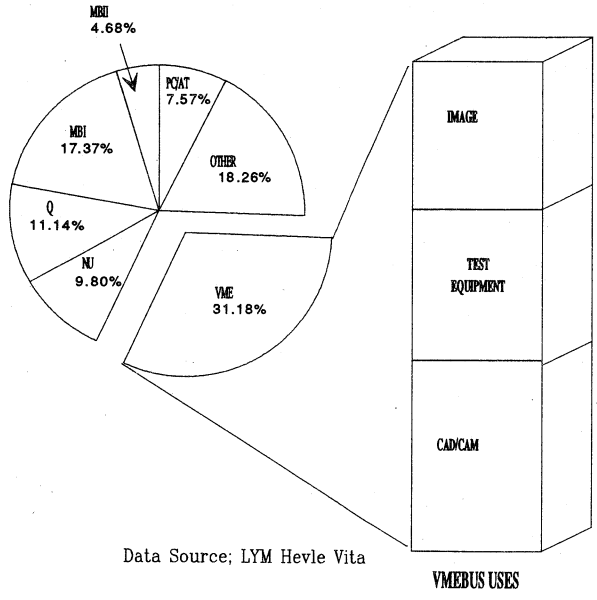


Figure 1.1 Board Market by Dollar Size

With rapid advances being made in the field of microprocessors, especially those employing the RISC instruction set, performance previously available on super-minis is now affordable at micro prices. To capitalise on this performance potential data bottle necks like the backplane need to be enhanced at a similar pace. Current backplane standards have now reached the point where they are the limiting factor in true high performance systems.

For example when VMEbus was introduced, with its 32-bit data bus, by Motorola, Mostek and Philips/Signetics in the early 1980's it was more than a match for the current 16-bit MC68000 processor. The 32-bit address bus allowed upto 4Gbytes of memory to be addressed, the MC6800 could only address 16Mbytes. Furthermore VMEbus could support data rates of upto 40Mbytes/sec whilst state of the art processors were tied 10 Mbytes/sec. The same was true for the next generation of processors, MC68020, which offered 32-bit address and 32-bit data - VMEbus had more than adequate bandwidth. However with the advent of the new RISC processors, the 25MHZ MC88000, the tables have turned, with VMEbus unable to do the 17 Mega Instructions Per Second (MIPS) justice. This trend is likely to continue as ECL processor version emerge with 100 MIPS capability.

The above illustration was based on VMEbus but the same can be said for other buses like the Intel biased Multibus II.

Futurebus+ is however more than a match for the performance requirements of not only todays RISC processors but the next generations also. In addition to the advantages shown in the foil Futurebus+ offers the following features;

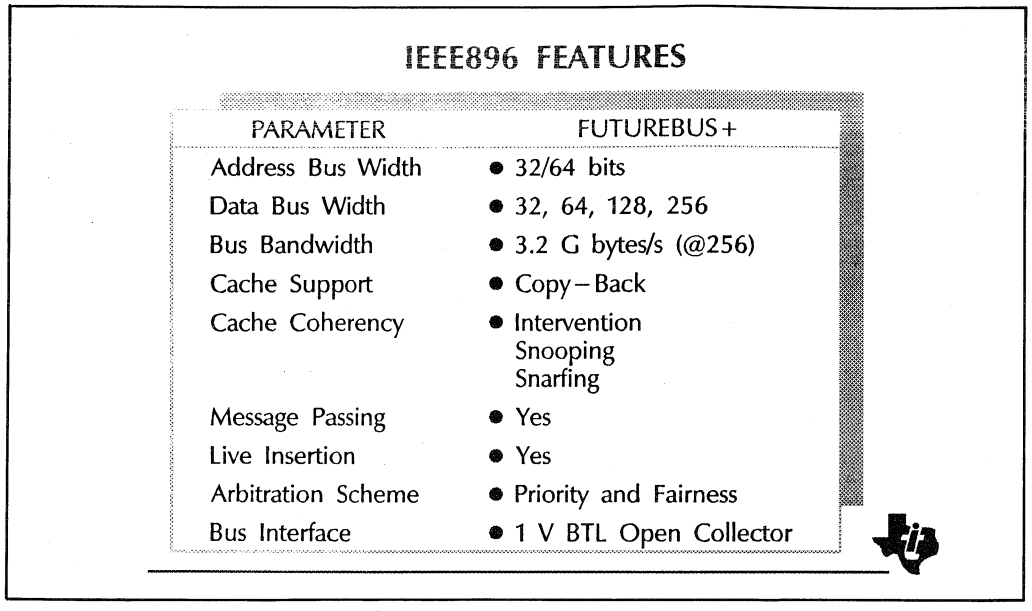


Figure 2 - IEEE 896 Features

0 High Data Transfer Rates

0 Cache Support

0 Message Passing

0 Fairness and priority arbitration schemes

0 Live Insertion

0 Backplane Transceiver Logic

These points are now discussed in more detail;

Transfer Data Rates

The the theoretical data rate of Futurebus+ is 100 M transfers/sec (3.2 Gbyte/sec) over a 256-bit data bus which is ten times greater than current backplane technology , which operates at 10 MTransfers/sec. Note the term mega transfer/sec is now used, FB+ is scalable from the standard 64-bits down to 32-bits and upto 128 and 256-bits. Specifying bus speed in terms of byte/sec does not take into account bus width. For example, a 25 Mtransfer/sec rate moves 100M byte/sec over a 32-bit bus, while the transfer speed is 200 Mtransfer/sec over a 64-bit bus. Even with the 32-bit option a transfer rate of 25 M Transfers/sec (100 M bytes/sec) is achievable.

Cache Memory

A technique often used to squeeze performance out of a system is to use cache memory. Cache memory is a localised memory, usually of small size but quick to access, used to store frequently used data. The processor accesses this localised memory without using the backplane. Accessing the backplane always costs bus bandwidth, since in times of heavy bus traffic the host may have to enter into time cosuming arbitration routines to gain ownership of the bus.

Simple caching occurs when the host retrieves data from shared (global) memory and then makes a copy into his own cache for future use. This can cause problems in a multiprocessor environment, because the host could modify the content of its cache memory without notifying or altering shared memory. The result is that shared memory contains stale data, and will not be current when cached by other processors.

VMEbus contains a feature called location monitor, which sets a flag when shared memory had been overwritten. The on-board cache controller then can invalidate all cache copies of this data. This technique, called *write through* , is fine providing each processor always writes to shared memory instead of cache, this results in high bus traffic. To reduce the amount of bus traffic most RISC processors have incorporated a *copy-back cache* routine. Copy-back caching processors access cache memory and update global memory only when they need the cache space for other use. This is the most efficient use of cache memory, however the possibility of the global memory containing stale memory still exists. Ensuring every location has uptodate memory is called cache coherency.

The Futurebus+ Cache Solution

Futurebus provides comprehensive support offering both cache coherency and message passing.

Cache coherency occurs when all cache memory locations and the global memory contains the same valid copy of memory. The Futurebus+ cache coherency scheme follows the MOESI model (Modified, Owned, Exclusive, Shared, Invalid) which uses a method called intervention to ensure cache coherency. The cache type used is copy-back, to overcome the problem previously discussed, ie stale memory, Futurebus+ employs two methods, *snooping* and *intervention.*

The Futurebus+ caching protocol requires that before any cache overwrite can occur it must first seek the permission of all other caches that have cached the same location. For simplicity lets call the unit with modified cache location 'M' (M for modified), all other cache locations will be called location 'O' (O for other). This is achieved by the generation of a special bus transaction which indicates the address of cached data from global memory. All cache coherent modules must monitor this line in a mode called *snooping*, ie they snoop the cache transaction line. If they detect an alteration to cache they then flag this by altering their tag associated with that cache value. This tag now invalidates its own cache value forcing the processor to access global memory and not the cache.

Whilst the processor is prevented from using its cache the contents of global memory have still not been updated. This is accomodated by using *intervention* . When a processor with an

invalidated cache memory (O) tries to access global memory the module with the modified cache (M) intervenes. By intervening the processor from location 'M ' prevents 'O' from accessing global memory and routes its own valid copy onto the futurebus backplane. One final term used with Futurebus+ cache terminology is *snarfing* . Snarfing while it doesn't contribute to cache coherency is extremley useful in reducing bus traffic. The handshaking protocols used in futurebus allow snooping boards, such as discussed above, to copy any data being read from or written to global memory. This is snarfing and it eliminates wasted time in accessing locations which have been recently updated.

For more demanding applications Futurebus+ supports a hierachical cache protocol. Put simply this uses all of the above techniques to maintain cache coherence between multiple backplanes.

Message Passing

Message passing is basicaly just that, ie a scheme which allows processors to send messages to each other. Message passing uses the same lines used for cache transfer.

Manufacturer Independent

Futurebus+ is not locked into any one processor, as is VMEbus (Motorola) and Multibus II (Intel), thus designers have much wider design options. Moreover the development of Futurebus has been a *joint development* between not only semiconductor giants but board /connector makers, computer manfacturers and the academic community.

This is probably the sole reason why Futurebus is so elegant a solution. It's designers started with a blank sheet and were not inhibited by trying to mould the system around any particular processor option. Futurebus+ is an IEEE sponsored standard, some of the member companies are; Texas Instruments, National Semiconductor, Signetics, Ferranti, BICC - VERO, DU-PONT, ITT-Cannon, U.S Navy, Hewlett-packard, Digital Equipment Corp and ABB of Sweden.

VMEbus and Multibus II See the Light (Enter thePlus in Futurebus)

After much debate two key organisations in the 'Bus Wars' VITA (VMEbus International Trade Association) and the MMG (Multibus and Manufacturers Group) announced their intent to follow Futurebus as their next logical upgrade. This announcement made in 1989 gave new direction and much needed support to the Futurebus camp which has led to a more practical solution, which will be compatible (via bridges) to both Multibus and VMEbus. This is basically where the '+' in Futurebus comes from. Early publications of Futurebus in 1987 are now redundant, with Futurebus+ being the only valid version.

Technology Independent.

Futurebus+ has made provision for both synchronous and asynchronous data transfer. The types supported are; Asynchronous (compelled), low speed synchronous (low speed packet transfer) and high speed synchronous (high speed packet transfer), it is the high speed packet transfer using 64-bit frames which gives Futurebus+ its highest data transfer rate. However the asynchronous protocol is the main workhorse of the Futurebus+ sytem. This means the timing of the data transfer is entirely determined by the transmitting module and receiving

module taking part in the transaction. Transactions involving faster modules can exchange data at their own capacity. Hence data transfer can take place at the speed of the slowest module. This is the independence of futurebus+, ie the sytem is not limited at design to a particular technology. Thus Futurebus+ systems will be able to improve along with technology .

Furthermore Futurebus+ does not use a central clock as in the Multibus II synchronous protocol. Using a central clock, ties all transactions to the speed of the clock irrespective of the modules data rate capability. Multibus II has 10 MHZ clock.

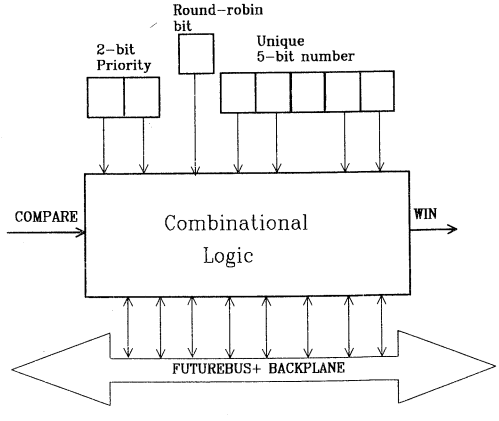
Arbitration

Arbitration is a method by which modules compete to gain ownership of the bus, bus mastership. Common schemes adopted are *priority* and *fairness*. In priority, each module in addition to its geographic address is assigned a priority number. The arbitration controller would then, via some combinational logic, arbitrate and award bus mastership to the module with the highest priority. The fundamental problem with this scheme is that lower priority modules could be starved of bus access, bus starvation. This is overcome by using fairness. Futurebus+ uses a round robin technique which basically arbitrates by offering bus mastership on a descending priority basis, ensuring that higher priority modules get bus mastership first but that all modules will eventually get a turn. Employing strict round robin arbitration creates problems too. Whilst it prevents bus starvation it does not take into account that some boards need quicker access to the bus than others.

Futurebus+ adopts the advantages of both, it assigns a few priority levels and than grants bus mastership on a round robin basis within each priority level.

In addition Futurebus + also features idlebus arbitration, which allows a module quick access to the bus without taking part in an arbitration routine -providing no other module requires bus access.

Figure 1.2 shows simplistically how fairness and priority arbitration is implemented. The most significant 2-bits represent 4 priority levels, the remaing 4-bits contains a round robin bit followed by a unique 5-bit number which is assigned to each module.



Figue 1.2 Futurebus+ Arbitration

Live Insertion or 'Hot Swop'

Another distingushing feature of Futurebus+ is the ability to insert or withdraw modules from the bus while the system remains powered. This is of paramount importance when multiple modules are used such as in military applications where equipment down time should be avoided.

The Futurebus+ Standards

The high and 'future proof' performance of the Futurebus+ specification is not only due to improvements in the logical layer but in the electrical specifications and mechnaical specifications to. This and more is contained within thirteen seperate specifications which are as follows;

Standard	Description
P896.1	**Futurebus+ Logical Layer, Includes signal names and the interaction of those signals.**
P896.2	**Futurebus+ Physical Layer, Includes board sizes and pinouts.**
P896.3	**Futurebus+ Systems Guide, Design guide to facilitate faster Futurebus+ implentation.**
P1101.1	**Futurebus+ Core Mechanical specification.**
P1101.2	**2mm connector convection cooled system specification.**
P1101.3	**2mm connector, conduction cooled system specification.**
P1014.1	**VME to Futurebus+ Bridge.**
P1156	**Environmental specifications.**
P1212	**Control and Status Register (CSR)**
P1296.2	**Futurebus+ to Multibus II bridge.**
P1394	**Serial Bus.**
P1301	**Metric mechanical Specification.**
P1194	**BTL electrical specification.**
P1194	**the BTL electrical specification is the subject of the next foil.**

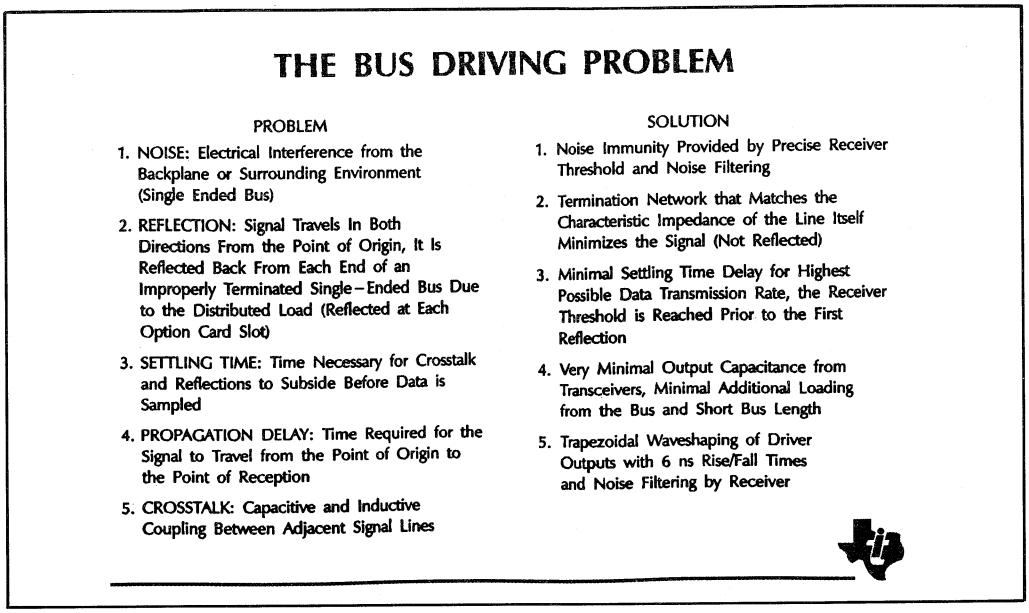


Figure 3 - The Bus Driving Problem

In a high performance systems, having high speed processors is not enough, the interface circuitry and the bus medium need also be considerd.

Futurebus+ faced this problem head-on by firstly acknowledging four major problem areas, collectively known as the 'bus driving problem' and by seeking ways to lessen their effect. The problems to overcome are;

0 Signal reflections
- **Caused by transmission line effects**
- **Each plug-in module adds a capacitive load to the bus**

0 Bus delay
- **Settling time**
- **Propagation delay**

0 Crosstalk

0 Noise

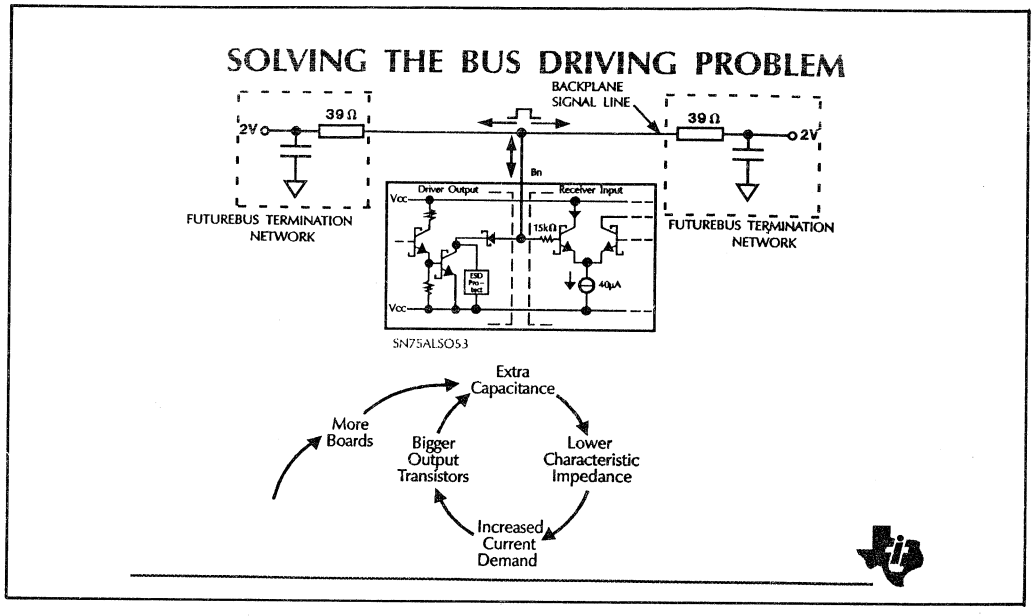


Figure 4 - Solving the Bus Driving Problem

The Backplane Behaves as a Transmission Line

One thing often overlooked is that the backplane is in fact a transmission line. A good rule of thumb states that a medium should be considered a tranmission line when the round trip propagation delay (2tpd) is greater than the device rise time (t_T).

$$2tpd >> t_T \quad (10\ tpd >> t_T \text{ provides a safty margin})$$

By applying this test to a simple application which uses the SN75ALS056 octal transceiver, t_r of 3 ns (typ), to send a signal over a backplane with tpd = 20 ns, it is quite clear that the backplane should be treated as a transmission line.

Consequently the first departure from normal backplane operation is to terminate the backplane in its characteristic impedance, this helps reduce reflections along the bus maximising the bus speed. The valve of 39Ω represents a compromise between the valve needed for a lightly and heavily loaded backplane.

The maximum transfer rate between any two modules is simply determined by the sum of the response time of the modules plus the bus delay. The module rise time is relatively easy to fix, with the current capability of the SN75ALS series more than adequate, however the bus delay is another matter. Especially since its not only a function of bus loading but the way in which the loading is distributed. There are two component parts to bus delay, the settling time and propagation delay. Settling time is the time required for reflections and crosstalk to subside and can be reduced by correct termination of the line as discussed below, this is usually several times larger than the propagation delay.

More Boards More Capacitance

Any board inserted onto the backplane will contribute a capacative loading, which since the bus is a transmission line must be treated as a distributed parameter. This additional load requires a greater current drive from the bus driver (transceiver). This seems reasonable, until you consider that increasing the drive capability of a semiconductor often leads to an increase in the area of the output drive transistors. This increase in area causes an increase in the drivers output capaciatnce.

This vicious circle is known as the bus driving problem and is illustrated in figure 2.1, its theory is proven below;

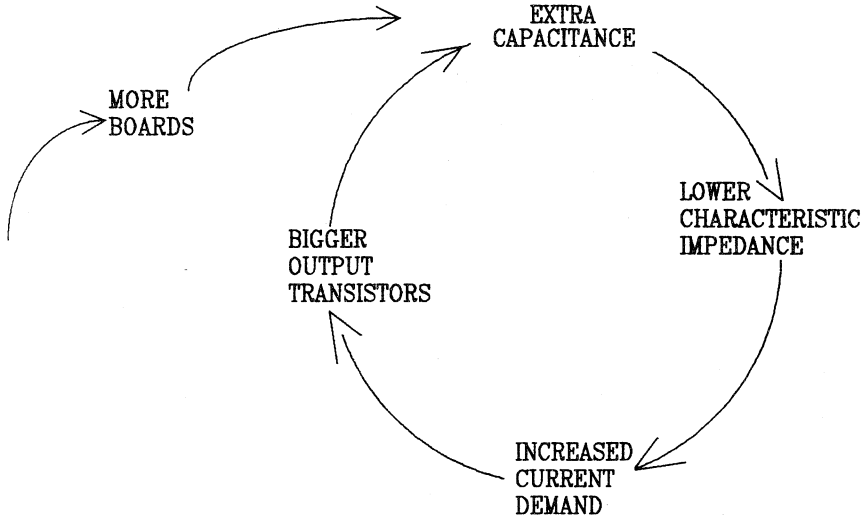


Figure 2.1 The Bus Driving Problem

Consider an unloaded backplane of characteristic impedance ZO and propagation delay tpd.

$$Z_O = \sqrt{L/C}$$

$$t_{PDO} = 1\sqrt{LC} \qquad 2.1$$

Where l = bus length, L = distributed inductance (per unit length) and C = distributed capacitance (per unit length). These valuse can be calculated for a typical 896 microstrip backplane (calculation not shown) giving $Z_O = 100\ \Omega$ and $t_{PDO} = 5.6$ ns/m

These values are for an unloaded backplane. However we have to take into account a loaded backplane with plug-in cards contributing to the capacitive load. Therefore the values of Z_L and t_{PDL} are now given by formula 2.2, where CL is the disributed load capacitance per unit length.

$$Z_L = Z_O \sqrt{1+(C_L/C)}$$

$$t_{PDL} = t_{PDO} \sqrt{1+(C_L/C)} \qquad 2.2$$

The typical distributed capacitance, C, of the unloaded backplane is approximately 66 pF/m. In addition to this however the plated through holes and trace capacitance must be considered. This can ammount to as much as 5 pF for the through holes and a further 3 -5 pF for pcb traces per card slot . However by far the most significant contribution can come from the transceivers themselves which for a standard TTL device can be in the range of 10 to 22 pF. This for a Futurebus+ system with 15 slots can add upto 1570 pF/m. Therfore using formula 2.2 we can see that the characteristic impedance has dropped from 100 Ω to 20 Ω, similarly the propagation delay has increased from 5.6 ns/m to 27 ns/m.

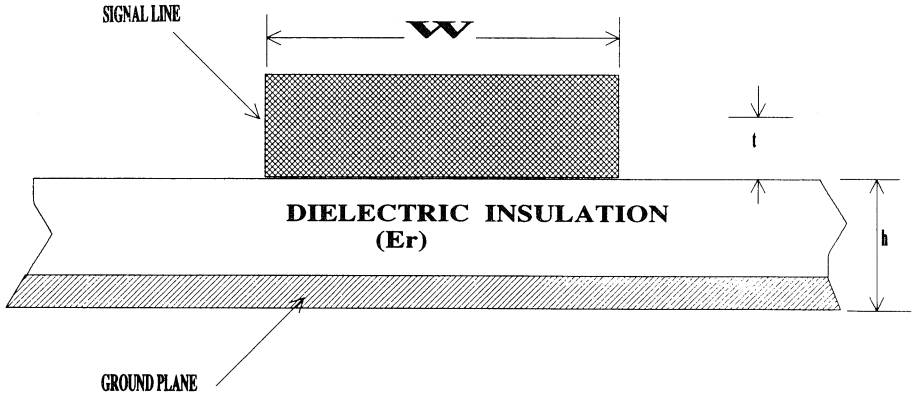


Figure 2.2 Construction of a Typical Backplane

The effect of the propagation delay is obvious, the lower characteristic impedance is a little more difficult to understand. A lower characteristic impedance is is harder to drive demanding greater current output from the transceivers output stage.

This proves our original assumption, the 'bus driving problem' of figure 2.1.

The extra current required in this case can be calculated for a TTL driver with a typical voltage swing of 3 volts . In this example the driver is mid way along the backplane, as in the foil. This halfs the characteristic impedance as the driver now has to drive current to both ends of the bus. Using a standard TTL driver with a typical voltage swing of 3 volts the current demanded of a loaded backplane can be calculated;

$$I_O = 3\ V / (Z_L / 2) = 300\ mA \qquad 2.3$$

A TTL driver with a 300 mA drive capability is not a practical solution. The alternative is to use a a standard 50 mA driver, but several round trip propagation delays will be required before the receiver threshold is reached, this obviously is at the expense of bus bandwidth.

Quite clearly the root cause of the problem is the capacitance, reduce this and the problem is lessend. This is how the Futurebus+ spec P1194 solves the problem. As discussed before the biggest contributory factor is the capacitance introduced by the transceiver. *P1194 specifies that the maximum capacitve loading offered by the transceiver must not exceed 5 pF.*

This increases Z_L to 30 Ω (by equation 2.2) which in turn reduces the current drive demanded to 50 mA (equation 2.3). Also from equation 2.3 we can see that the propagation delay has also been reduced to 19 ns/m.

The SN75ALS05X series of devices from TI all feature a reverse biassed schottky diode with a series capacitance of about 2 pF. This, when connected in series with the collector emitter output transistor yields a total capacitance of approximately 3 pf. Added to the receiver input capacitance of 2 pF the total transceiver loading capacitance is kept below 5 pF.

This is just one of the features of the BTL, Backplane Transceiver Logic, specification which is the subject of the next foil.

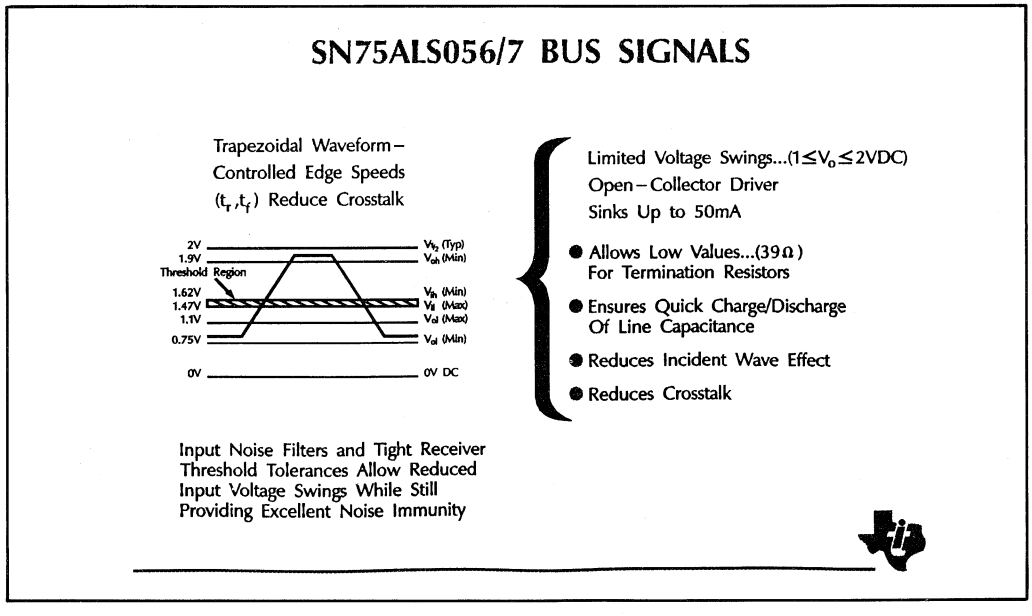


Figure 5 - SN75ALS056/7 Bus Signals

Backplane Transceiver Logic

BTL is an open collector logic family that uses a logic high of 2 V (Max) and a logic low of 0.7 V (Min), plus a tightly controlled receiver threshold switching voltage between 1.47 V and 1.62 V, see foil.

The first thing to note is the reduced voltage swing of 1 V not the normal 3 V expected of TTL systems. This reduced voltage swing along with tightly controlled receiver threshold voltage means that the initial step applied by the driver can cleanly cross the receiver threshold without having to rely on reflections. This again maintains a high bus through-put. Secondly having a low voltage swing also yields a power saving, which can be considerable when in a 32-bit sytem as many as 40 lines could be switched simultaneously.

Noise Margins

Having a lower voltage swing, may at first seem to result in lower noise margins when compared to TTL stystems. This is not the case, figure 3. 1, and in fact the more sensitive noise margin in the backplane bus, the voltage level below the receiver threshhold level is greater than that that offered by TTL; 720mV Vs 400mV.

The Futurebus+ receiver specification is greatly improved over TTL by utilizing very tightly controlled receiver threshold levels. The receiver thresholds are centered between the the low and high levels of the bus, 0.75 Vand 2 V. This threshold is confined between 1.62 V and 1.47 V which tracks the the high input level to provide a maximum noise margin with respect to the low and high signal levels on the bus.

The Futurebus+ receiver incorporates a noise filter to selectively reject crosstalk noise pulses of upto 8 ns in pulse width. This effectively provides a further increase in noise immunity.

Trapezoidal Wave Form

A concept well known to designers is that crosstalk, passing of noise to adjacent lines, is a function of the drivers output rise and fall times, dv/dt. Having recognised this fact, a problem arises since the requirement for high speed systems is fast transitional edges.

By using a driver with a trapezoidal output this can be overcome. The trapezoidal edge is a carefully controlled , slew rate limited, ramp. Which, although has a reduced transition speed between 10% and 90% of the output signal, the transition through the receivers narrow threshold region is not significantly impaired.

In summary, Futurebus+ BTL devices solve the 'bus driving problem' allowing a 50 mA driver to create a voltage steps which crosses first time through the receiver threshold without having to wait for reflections. The smaller voltage swings plus the symmetrical receiver noise margins provide considerable increase in data integrity. Crosstalk is a function of the amplitude of the active signal, Futurebus+ has a lower active signal an a trapizoidal output thus crosstalk between adjacent lines is much reduced.

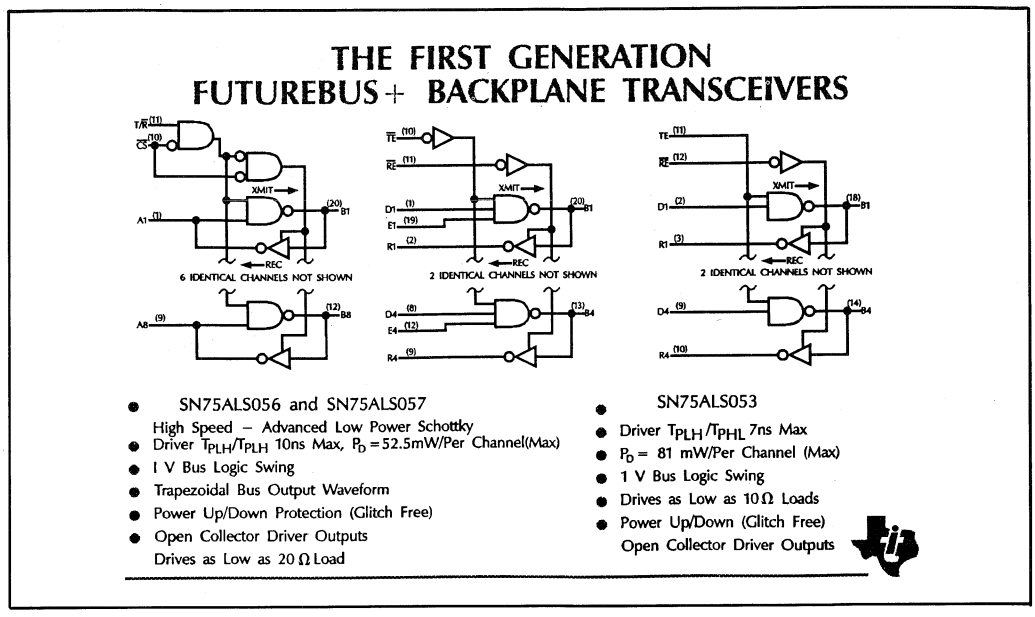


Figure 6 - The 1st Generation Futurebus+ Backplane Transceivers

The requirements for a BTL transceiver has now been well developed. TI has devices to fulfil the requirments of the P1194 BTL specification.

Presently there are three offerings, all developed using the advanced low power schottky process, the *SN75ALS056* octal, the *SN75ALS057* quad and the *SN75ALS053* turbo quad.

The 057 is a 4-channel device with an indepedant drive (DN) input and receive output (RN) controlled by separate driver enable/disable. The 056 is an 8-channel device which is controlled via a chipselect and single driver / receiver enable disable pin. Both are housed in a 20 pin-package N or DW package.

These transceivers feature open-collector outputs with a series diode to reduce the capacitive loading on the bus. By using a 2 V pull-up voltage the output signal swing is approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs generate a trapizoidal waveform that reduces crosstalk between adjacent channels. The 056/057 are capable of driving an equivalent dc load as low as 20 Ω, while the 053 with increased output current can drive a 10 Ω load.

Due to the ALS technology all devices benefit from low power and high speed operation. The power dissipation of the 056/057 is 52.5 mW per channel while the 053 is 81 mW per channel.

The 056/057 has a maximum driver propagation delay of 10 ns, while the 053 has a driver propagation delay of 7 ns. The driver rise time of the 053 is 5 ns max, with a skew between channels of 1 ns max.

All receivers have a precission threshold set by an internal bandgap reference to give an accurate input thresholds over both time and temperature variations. The SN75ALS053 is shown in a test system in the next foil.

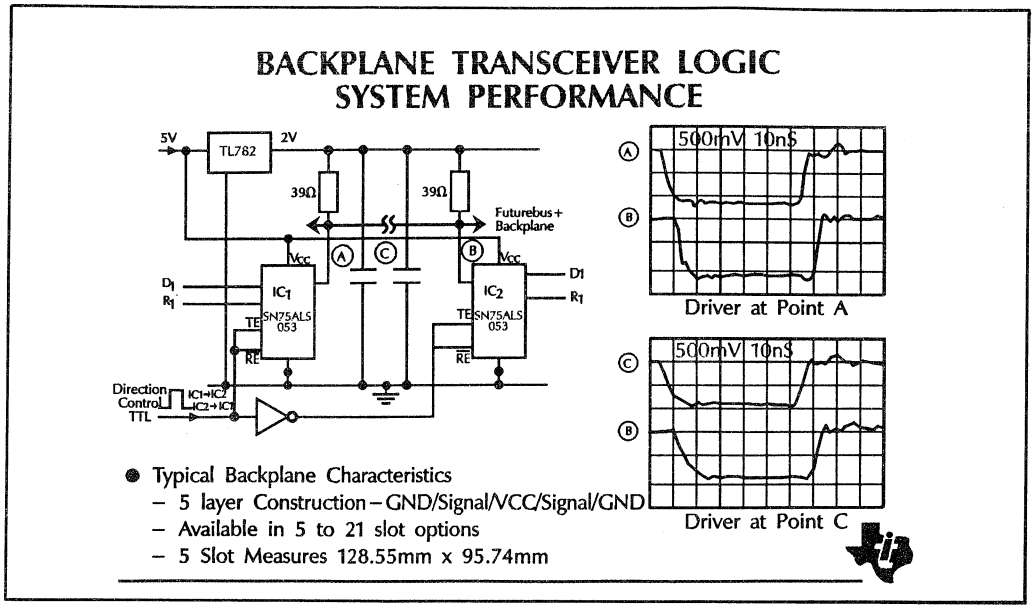


Figure 7 - Backplane Transceiver Logic System Performance

Simply this foil shows the BTL signals on the backplane. The test circuit was set upto allow bi-directional control of the SN75ALS053 devices.

A logic signal is applied to the TE and RE inputs of for IC_1 is inverted and fed to IC_2. This forms the direction control for the flow of data. A logic high to IC_1 results in the signal flow from IC_1 to IC_2.
The line is terminated into 2 V via two termination resistors of 39 Ω. The voltage is supplied by a TL782 regulator.

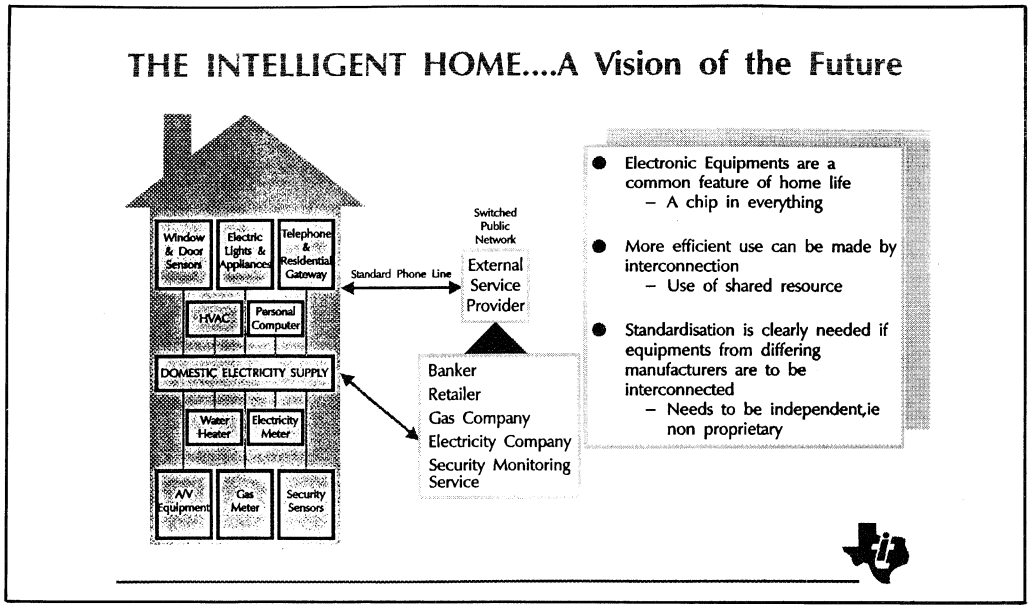
The backplane is a 5 layer multilayer, plated through hole construction with interlaced ground, V_{CC} and signal lines. This type of construction ensures a constant characteristic impedance of the signal lines with respect to the ground planes reducing crosstalk and signal skew.

Backplanes and connectors are available from many different manufacturers and are generally offered in 5, 10 15 and 21 slot options. Several of these manufactures also offer a Futurebus+ terminator which plugs into spare sockets on the backplane to provide the necessery termination voltage and termination resistance.

The graphs show the nature of the BTL signals on the backplane.The top trace in each figure is the driver output whilst the bottom trace represents the input to the receiver. The top figure illustrates the case when the bus is driven from the end, while the bottom figure shows the situation when the bus is driven from the middle. Note in this case the driver will actually see two loads one to the left and one to the right.

Future Developments.

Texas Instruments is committed to the Futurebus + Standard. It has a team of experienced engineers exclusively dedicated to the design and promotion of Futurebus + Products. The second generation of tranceivers, 9 channel latching transceivers, are already available in sample quantities and development work of the Futurebus controllers is in an advanced stage.



CEBus

Figure 1- The Intelligent Home...A vision of the Future

This section will address TI's involvement in what could turn out to be one of the major markets of the 1990's - **DOMOTICS**. In particular it details a brief outline of one of the many emerging standards which are set to serve this market, the EIA CEBus.

There is currently a great deal of activity and indeed investment aimed at the domotic market. All sectors are actively involved, from semiconductor companies, white / brown goods manufactures, electricity boards, industrial and home building companies. All in all, no one company invoved in these industries can afford to ignore the standard if they are to maintain a competetive position in their respective market.

Put simply domotics allows the interconnection of all electronic equipment within the home, permitting use of shared resource and offering the home owner complete control over the home environment

A CEBus Scenario

One need only look at how electronics has pervaded home life, security systems, audio / visual equipments, heating / ventilation control white goods to name just a few to see how common a feature of home life electronics is. However the information stored in each item is localised and cannot be distributed to other equipments, surely the next logical step is to interconnect this eqipment making use of common information.

A typical scenario could be as follows; The electricity board has several electricity tariffs. These are used to evenly distribute the load demanded, so that the peak demanded is flattend and the off-peak demand is increased. This is load management and is not a new concept for

the electricity boards, however up until now multi rate tariffs have not been practical. One particular low-rate tariff is guaranteed for a period of 4 hours in every 24 hours, however the timing is not guaranteed and is dependent upon the boards loading. CEBus or other such domotic standard is used to make use of this variable low tariff electricity in the following manner; The home owner would pre-programme all home appliances which could make use of this tariff, ie appliances which are not time dependaent, dish washers, storage heaters, water heaters, baterry charged equipments and washing machines etc.
The electricity board then signals using a CEBus packet to the domostic electricy meters that low-tariff is available. These in turn will signal, again using a CEBus packet, to the home appliances to turn them on.

This is just one application for the intelligent home, there are many more which are limited only by your imagination.

Furthermore standardisation is key to the successs of domotics. The reason for standar disation is clear when you consider the multi-disciplines required to effect an intelligent home, homebuilders, semiconductor companies, electricity boards, consumer manufacturers...etc. All must have clear unambiguous detailed information from which to design and manufacture products.

Also, a some what lesser requirement is for the standard to be non-propriety, independent from any particular manufacturer, to allow all manufacturers equal access to compete in an open market.

Market Potential

If your still not convinced of the market potential for domotics then consider the market size;
144 Billion homes in Europe alone, if each household contributed just 2% of its house value to implementing an intelligent home, that equates to 4 billion dollars worth of semiconductors for 1995.
A vision of the future is upon us now.

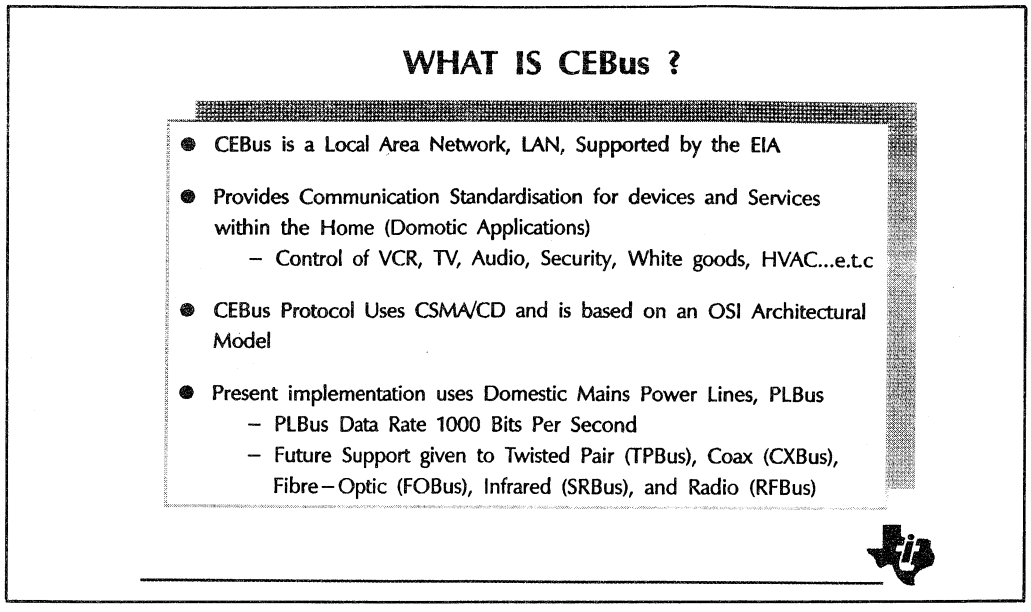


Figure 2 - What is CEBus?

Having established the need for some kind of domotic standard , we can now look at one such standard - the Consumer Electronics Bus, CEBus.

The CEBus standard provides a common networking protocol for two-way communication over multiple media, including existing in-house power lines, twisted pair wiring, co-ax, fibre optics, RF and infra red. CEBus is an EIA, Electronics Industries Association, sponsored standard, and as such operates independently from any manufacturing organisation, ie non-propriety. Having said that, the active membership is made up of some 50 or more companies from all sectors of industry, with over 2000 companies monitoring the standards progress. Although a U.S organisation its importance cannot, and should not, be overlooked as a major force in Europe, more so for companies who export to the U.S. The EIA has a proven track record of setting such standards such as international standards like RS232 and RS485 etc.

Four Years in the Making

CEBus has been more than four years in the making, and is now out for final ballot. A fully released specification, IS-60, is expected by August 1990. In any case the protocol is highly unlikely to change , so system designers can already use the standard. The item most likely to change will be the physical layer which details the modulation method for sending information over the network. The standard currently specifies an ASK, on-off keying, technique, however general thinking is that the spread spectrum technique offers a more elegant solution permitting faster data rates with higher noise immunity. It is possible that a finalised specification will contain the spread spectrum technique and not the current ASK.

CEBus is best described as a LAN , Local Area Network, similar in construction and operation to other LANS such as Ethernet token ring...etc. However rather than just providing for the interconnection of computers to their peripherals, CEBus allows intelligent equipment

within the home to communicate over the CEBus medium.

CEBus uses the OSI Model

To simplify and speed the adoption of CEBus The OSI, open systems interconnect, model is used. The OSI model is partitioned into a series of seven layers (some of which may be null), which serves to simplify the overall design complexity. These layers are hierarchical with each layer built upon its predecessor. Each layer provides a defined service which is shown in figure 2.1. The method by which each layer provides the function is not important, what is important however is the way in which each layer communicates to the next layer. It is this feature which permits manufacturers of such diverse equipment, ranging from simple light switches to security systems to build products that can communicate with each other.

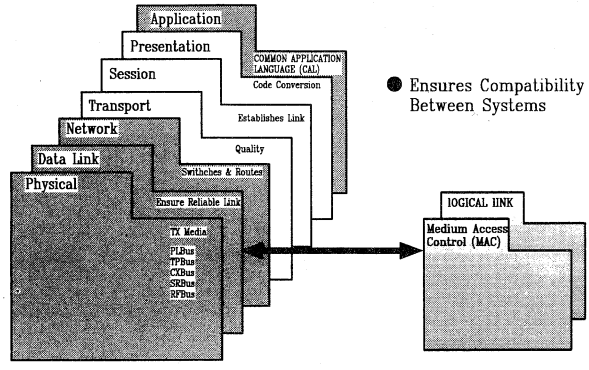


Figure 2.1 The 7 Layer OSI Model

Further more the adoption of a peer protocol such as CSMA/CD makes for a standard which is much more robust and versatile than alternative standards there is a much higher chance of messages getting through without error. The carrier Sense, Multiple Access with Collision Detection protocol is well known to Ethernet users, and basically is a mechanism to ensure that there is no data collision over the network, nodes similtaneously sending data. Further more the CEBus protocol allows for data checksums giving error detection and the re-transmission of erroneously received or unacknowledged packets.

A typical CEBus message packet has a structure as shown in figure 2.2

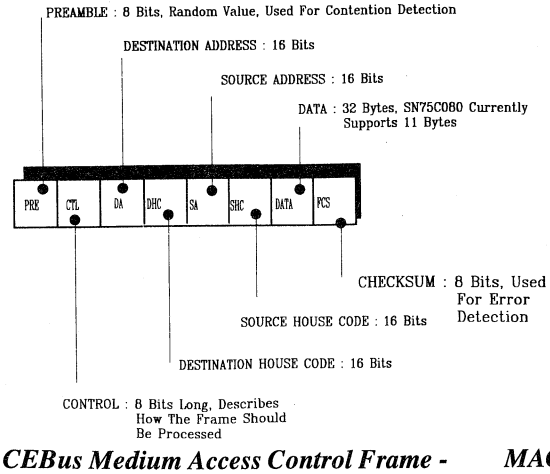


Figure 2.2 The CEBus Medium Access Control Frame - MAC

In its present implementation the CEBus medium uses the domestic power line. Information is modulated using amplitude shift keyed, ASK, technique to modulate a 120 kH_z carrier onto the mains signal. This results in a data rate of 1000 bits per second which can be used to send control information short packets at low data rates.

For more data intensive communication or nodes requiring larger bandwidths, ie audio / visual applications other types of medium are embraced by the CEBus standard. Examples of which are twisted pair , TPBus, coax, CXBus, fibre optic, FOBus, infrared, SRBus and radio, RFBus.

CXBus is expected in draft form by August 1990.

All things being considered CEBus is the most elegent solution for Home Automation and is by far the most advanced in terms of published specifications and semiconductor implementation.

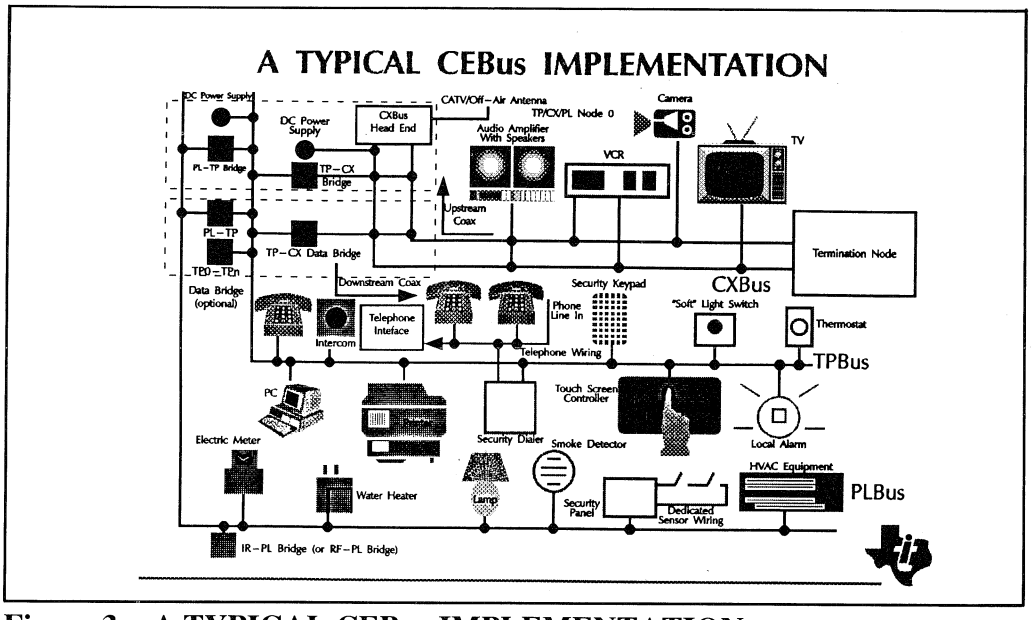


Figure 3 - A TYPICAL CEBus IMPLEMENTATION

Although rather complicated this foil serves to illustrate how a typical CEBus network would be implemented. Devices requiring simple on/off control functions or equipments that are not speed dependent, eg washing machines etc can be connected via the PLBus. Equipments which either need to operate at higher data rates or which need wider bandwidth ie telephone systems, 20 H_z to 20 kH_z, are connected via the twisted pair bus, TPBus. Alternatively, systems involving the transmission and reception of audio or visual information, such as television receivers, video recorders / cameras and CCTV systems will use the coaxial bus, CXBus. Remote control for equipments such as audio / visual, light dimmers etc can be effected via the infrared bus, IRBus.

The key thing to note with CEBus is that irrespective of the media involved *the protocol is common*. CEBus is a communications backbone and not a cluster based system as are the majority of competing standards. This means there is no need for complicated gateways between different equipment, the CEBus bridge is very simple.

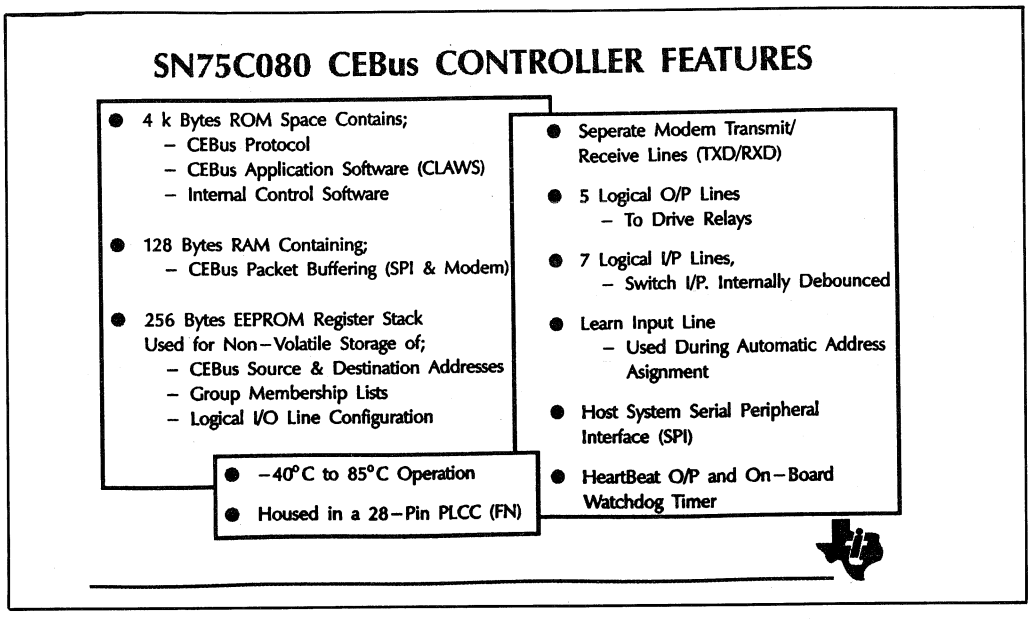


Figure 4 - SN75C080 CEBus CONTROLLER FEATURES

The SN75C080 controller is a general purpose interface for the EIA CEBus. Using this device allows the user to build a simple easy to use interface for the CEBus network, allowing communication with other similar devices. It is esssentially a dedicated 8-bit microcontroller which is implemented in high-performance 1.6 micron silicon-gate CMOS technology. The low operating power, wide operating temperature range and high noise immunity make the device highly suitable for operating in either the industrial or domestic environments.

The SN75C080 fully implements the CEBus data link layer protocol specification. Basic application requirements are supported on-chip while extended services may be implemented by the user.

On-Board ROM, RAM and EEPROM

The device features both ROM, RAM and EEPROM and is partitioned as follows;

4 k Byte ROM : Used to house the CEBus protocol, the application software and the internal operating code. The SN75C080 contains a simple application software, CLAWS[1], which allows the user to perform automatic address assignments and build communication relationships with other CEBus nodes on the network.

128 Bytes RAM : Used for CEBus packet buffering.

256 Bytes EEPROM: Reserved for non-volatile storage of CEBus source and destination addresses, group membership lists and the logical I/O configuration.

[1] CLAWS :- CyberLinx Application Wall Switch

Serial or Parallel Communication with the Host

Communication with the application host controller can be achieved in one of two ways, in parallel via the twelve logical inputs and output lines or serially via the SPI.
Seven lines are are assigned as sensor inputs used to detect switch closures or logic signals and five lines are assigned as actuator outputs to drive relays, triacs, or other logic compatable inputs. Additionally there is a learn input which is used by the CLAWS application to automatically assign unit addresses.

The SPI provides an efficient method of serial communications which can be used to communicate to simple shift register type devices. Such devices may be display drivers, A/D converters etc or with microcontrollers such as the TMS7000 series and TMS370 series.

To protect against software failures the SN75C080 includes a watchdog timer and heartbeat output.

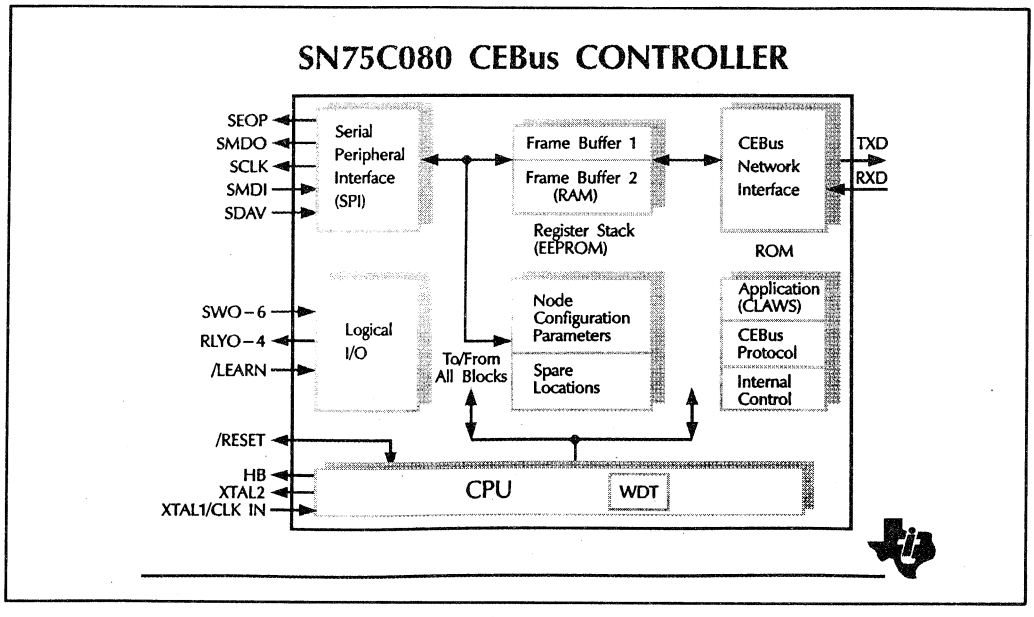


Figure 5 - SN75C080 CEBus CONTROLLER

SN75C080 Architecture

The inter-relationship of the blocks previously discussed is now shown. Of note is the relationship between the 8-bit microconrtoller and its memory, also note the SPI signal pins , the logical input/output pins SW0-6 and RLY0-4, the learn input and the reset input. The device supports three types of reset, a reset on power-up, a logic low on the reset pin and watchdog time out.

Clock sources

The clock input to the SN75C080 can be either a 20 MH_Z crystal or ceramic resonator, the SN75C080 contains an internal oscillator circuit, or a 20 MH_Z logic-level squarewave with a duty cycle of approximately 50 %.

Communicating with the outside world

Communications to the CEBus network is via TXD and RXD pins. These interface directly to the medium modem, in this case the PLBus modem, SN75081.
The signal levels are defined by the CEBus pyhsical layer and are of the pulse width encoded, non-return to zero format, see figure 5.1.
The four symbols are;

SYMBOL	PULSE WIDTH	DEFINITION
One-bit	**1 ms**	**Encoded binary 1**
Zero-bit	**2 ms**	**Encoded binary 2**
EOF	**3 ms**	**End of field delimiter**
EOP	**4 ms**	**End of packet delimiter**

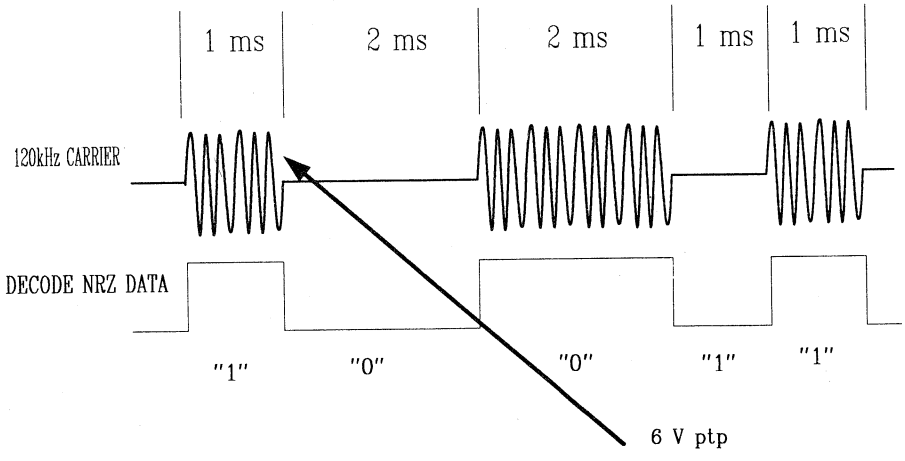


Figure 5.1 The PLBus Signals

When TXD is high, it is a command to the modem to place a carrier-on (superior) state onto the CEBus medium. When TXD is low, it is a command to for the modem to switch to carrier-off (inferior) state and not drive the CEBus medium. Similarly RXD is an input to the SN75C080 from the modem used to indicate the presence of a signal on the CEBus medium.

The Tried and Tested CSMA/CD Protocol

The SN75C080 monitors RXD to determine if the CEBus channel is clear and that no other node is transmitting before it begins to transmit its own message. While transmitting SN75C080 continues to monitor its RXD input to look for data collision with other nodes. If a collision is detected it will cease transmission (back-off) for a length of time determined by its priority and then resume transmission. When the TXD is high from the SN75C080 the modem must squelch (hold low) its RXD output. Otherwise the SN75C080 will consider a high on its RXD as a collision. This is the Collision detection function of the CSMA/CD protocol.

The Serial Peripheral Interface - SPI

As previously discussed the SN75C080 has two methods of communicating with the host application controller, via the logical I/O pins or via the SPI. We will now focus on the SPI;

The SPI is a synchronous serial I/O port which allows 8-bit data to be shifted into or out of the SN75C080 as serial bit stream at a clock rate of 40 kHZ.
The SPI has 5 lines over which it communicates, they are;

SCLK: **SPI clock used to control the data exchange to and from the host.**
SMDI: **SPI data into the SN75C080 from the host.**
SMDO: **SPI data from SN75C080 to the host.**
SEOP: **SPI end of packet. This is used as a handshake from the SN75C080.**
SDAV: **SPI data available. Used as a handshake from the host to the SN75C080.**

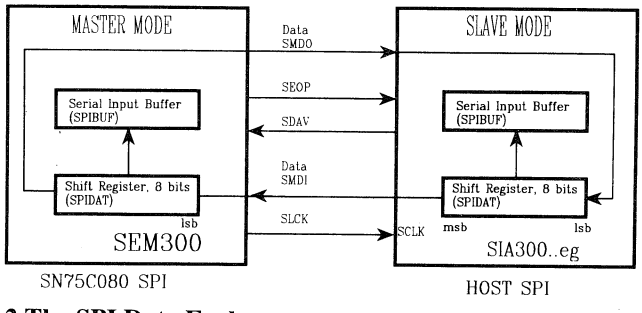


Figure 5.2 The SPI Data Exchange

SPI Protocol and message types

To send an SPI message to the SN75C080, the slave, first puts a message type byte in its SPI register and asserts SDAV. The SN75C080 responds to the interupt by clocking in the byte. It is examined and, if necessary for that type of message, futher bytes are clocked in. Each byte is transfered after the SDAV line is asserted.

When the SN75C080 wants to send data to the host it first drives SEOP high and begins to clock out its data. The host is expected to be always ready to accept data. The SN75C080 will drive SEOP low to signal it has sent the last byte of its packet. This is is how the host determines the length of the packet, which are of variable length. All other messages sent from the SN75C080 to the host are of a fixed predetermined length.

The SN75C080 SPI also offers a simple protocol which supports six basic message types;

R: Received frame message (from CEBus)
T: Transmit frame message (to CEBus, host provides header fields)
t: Transmit data message (to CEBus, SN75C080 provides header fields)
S: Status message (results of transmit operation)
E: Write EEPROM register message
e: Read EEPROM register message

More detailed information on the SPI operation can be found in the SN75C080 data sheet which is contained in the CEBus data pack LL116.

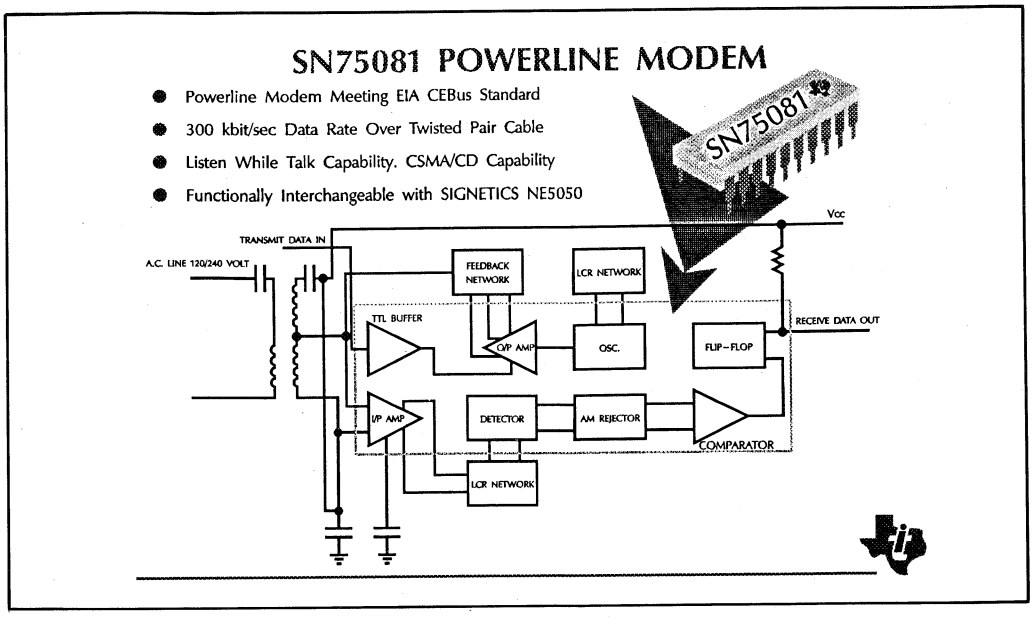


Figure 6 - SN75081 Powerline modem

The SN75081 is a modulator/demodulator (modem) for powerline, twisted pair and coaxial cable communication.The device is capable of operating at data rates as high as 300 kbit/s over twisted pair. However as the present revision of the CEBus specification calls for a powerline medium the SN75081 is used in its ASK powerline modem configuration. The device has 'listen while it talks' capability which allows CSMA/CD to be implemented. Put simply this means that the device is always in the receive mode, even when transmitting. Therefore the device can sense a collision on the network, and back off under the control of the SN75C080 controller. Further more the device is functionally interchangeable with the signetics NE5050 so making it suitable for a whole host of applications beyond CEBus.

Transmitter Block

The transmitter block includes a colpits oscillator, a carrier-on/off switch and a line output driver. The oscillator is a differential transistor pair. As such it can be configured as a colpits LC oscillator, as a pierce crystal oscillator or used with an externally applied input. The line driver is a class AB push-pull stage with the provision for external connection of a complementary transistor pair giving increased current capability.
By itself the SN75081 is capable of driving a consumer line impedance of 50 W, with the THD being less than 2%. By connecting external complentary transistors such as the TIP-31A and TIP-32A, 10 W industrial loads may be driven. With a complementary darlington transistor configuration 1 W industrial loads can be driven.

Receiver Block

The receiver has an amplifier, a limiter, an amplitude detector, an amplitude modulation cancelling stage an impulse filter and a SR flip-flop.
The receiver sensitivity is 1.5 mV (rms), which can be reduced by adjusting the turns ration of the coupling transformer or by inserting loss in the bandpass filter. The input amplifier/limiter

limits its ouput signal to 1.2 V (p-p), while the gain is 24 dB.

More detailed information on the operation and application of the SN75081 can be found in the SN75081 data sheet which is contained in the CEBus data pack LL116.

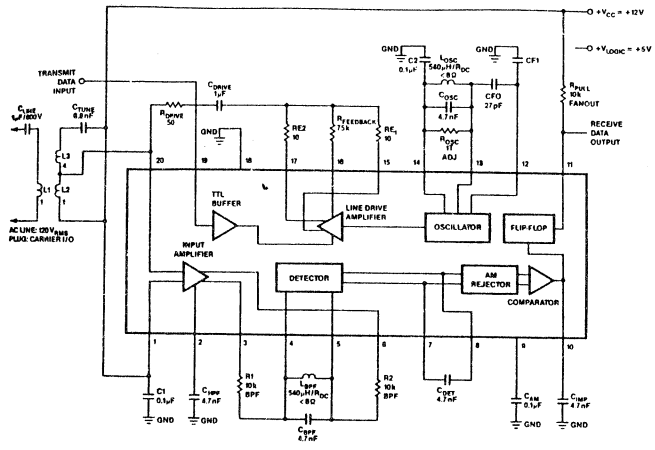


Figure 6.1 Typical application circuit for 120/277 V AC line

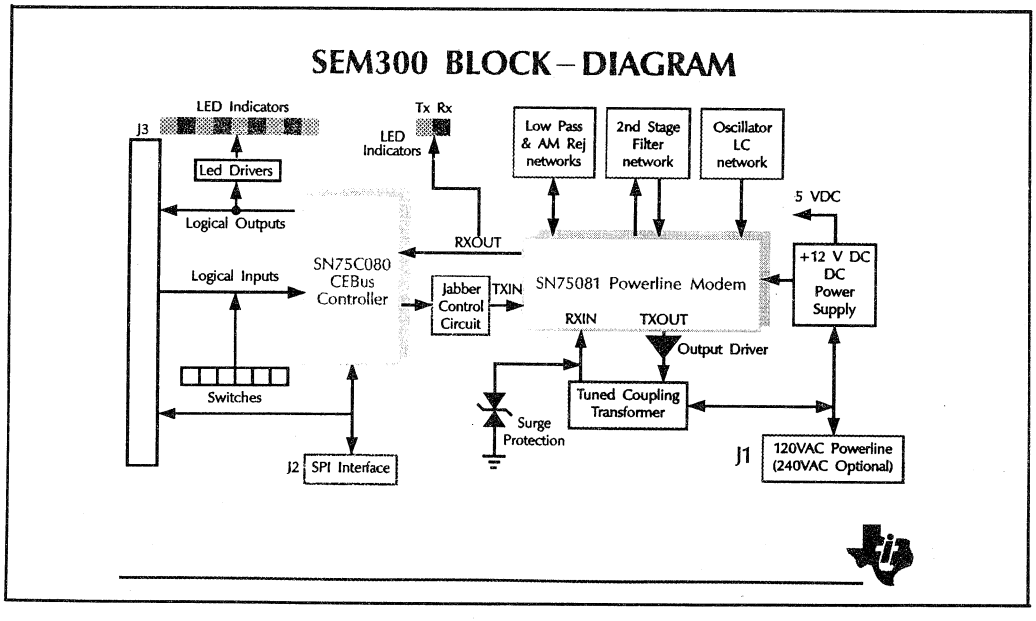


Figure 7 - SEM300 Block-Diagram

The Cyberlynx connection

To bring added resource to TI's development of products for the CEBus standard TI has a cooperation agreement with Cyberlynx Corp of the U.S. Cyberlynx, a software development company, has a proven track record in the domotic industry and has been a major player for the past four years.

The agreement allows for the joint development of products and software support for the CEBus standard. To date TI has developed the SN75C080 controller and the SN75081

power-line modem while Cyberlinx has developed the software code and two CE Bus evaluation modules, the SEM300 and SIA300.

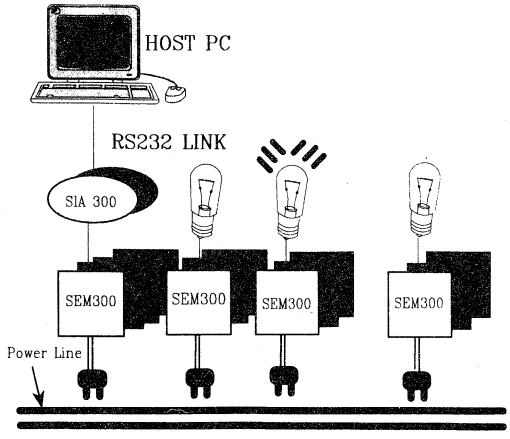


Figure 7.1 The SEM300 and SIA300 Evaluation Modules

The purpose of these modules is stated below;

0 Purpose of SEM300

- To allow the user to become familiar with the CEBus standard.
- Allow the user to quickly evaluate the SN75C080 and SN75081.
- Assure compatability between other CEBus products.
- Reduce product development cycle time.

0 Purpose of SIA300

- Provides user freindly interface between the user and the SEM300.
- Operates on PC under the DOS operating system.
- Allows the user to construct CEBus packets, observe received packets, monitor and log CEBus activity.

The SEM300 Block Diagram

The diagram shows the inter connection between the SN75C080 controller and the SN75081 powerline modem. Communication to the host is via J2 for serial SPI communication or via J3 for parallel communication. Connection to the CEBus medium is through the tuned coupling transformer and via J1 to the mains power supply. The output driver is formed by two complemtary transistors TIP-31A and TIP-32A. The logical I/O connector J3 is wire-ored with switches for the inputs and and LED drivers for the outputs.

The jabber control circuit is used to prevent a CEBus node from Hogging the CEBus network.If the jabber circuit detects 'talking' for longer than 1 second it disables the SN75081 powerline modem

TEXAS INSTRUMENTS

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